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The PC Handbook (Formerly The XT-AT Handbook)

For Engineers, Programmers, and Other Serious PC Users

John P. Choisser
John O. Foster

Sixth Edition

Now with more PCI, VL, PCMCIA, and SCSI data!

A Collection of Hardware, Software, and Firmware Facts on the PC-Compatible Family

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Sixth Edition

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INTRODUCTION

As we usually warn our readers, if you have an earlier edition of this book, you might want to consider keeping it. In order to make room for some of the new subjects in this Sixth Edition, we had to eliminate some sections. In particular, most of the XT-only sections are gone, and we have eliminated the hard drive types and the line drawing codes.

We've added or expanded other sections, most of which you have asked for: VESA VL bus, PC Card (PCMCIA) information, and more PCI (PCI is also the subject of its own handbook now) and Small PCI. We've also expanded and updated many other sections.

Whether you're a novice or an expert, we expect that you are going to find this book useful. If you're a novice, the contents are going to be a stimulating introduction to the inside goings-on that you will want to learn more about. If you are an expert, you will find this handbook to be a handy memory jogger. When the facts you need are buried in a manual in the other room, this book is in your pocket.

We intended this to be a helpful reference for both hardware and software information. These are the items that most often cause us to look for the manuals, whether we're hooking up a printer or hooking into the BIOS.

For additional information on any of these subjects, you should refer to the manuals and technical references for the computer and software you are using, or call the appropriate standards organization. You might find the phone number you need in the first section!

We want to continually improve this handbook, so please write to us if you spot any errors or think of any additional material we should include. We hope it will be as useful for you as it is for us. And many thanks to those of you who have contributed ideas and corrections! (Your new free handbook is on the way!)

1. Useful References

Here are some of the phone numbers we get asked for most often. If there are others you need or would like to see added to this section, please call Annabooks.

ANSI, 212-642-4900 (NY)

CardBus see PC Card and Yenta

FireWire (IEEE 1394), 512-305-0200

Global Documents (source of specifications such as ESDI) 800-854-7179

I2O (Intelligent I/O) SIG, 415-750-8352

IEEE Publishing, 908-981-0060

IDE try ANSI(?)

Miniature Card Implementer's Forum, 916-356-8607

PC Card (PCMCIA), 408-433-2273

PCI Special Interest Group, 503-797-4207

PC/104 Consortium, 415-903-8304

Plug and Play Association, 503-797-4244

SCSI try ANSI (?)

USB (Universal Serial Bus) Implementer's Forum, 503-264-8429

VESA, 408-435-0333

Yenta (CardBus),

and when all else fails

Annabooks, 11838 Bernardo Plaza Ct., San Diego, CA 92128-2414, 619-673-0870 or 800-462-1042. Also, you can use http://www.annabooks.com or info@annabooks.com.

2. ISA 62 Pin Connector

(Bracket End of Board)

	Ground	<	B1	A1	<	IOCHK*	
	Reset	<	B2	A2	<>	SD7	
	+5 Volts	<	B3	A3	<>	SD6	
	IRQ2/9	>	B4	A4	<>	SD5	
	-5 Volts	<	B5	A5	<>	SD4	
	DRQ2	>	B6	A6	<>	SD3	
	-12 Volts	<	B7	A7	<>	SD2	
	SRDY*	>	B8	A8	<>	SD1	
	+12 Volts	<	B9	A9	<>	SD0	
	Ground	<	B10	A10	<	IOCHRDY	
	SMEMW*	<	B11	A11	>	AEN	
	SMEMR*	<	B12	A12	<>	SA19	
	IOW*	<>	B13	A13	<>	SA18	C
	IOR*	<>	B14	A14	<>	SA17	O
	DACK3*	<	B15	A15	<>	SA16	M
S	DRQ3	>	B16	A16	<>	SA15	P
O	DACK1*	<	B17	A17	<>	SA14	O
L	DRQ1	>	B18	A18	<>	SA13	N
D	DACK0*	<	B19	A19	<>	SA12	E
E	BCLK	<>	B20	A20	<>	SA11	N
R	IRQ7	>	B21	A21	<>	SA10	T
	IRQ6	>	B22	A22	<>	SA9	
S	IRQ5	>	B23	A23	<>	SA8	S
I	IRQ4	>	B24	A24	<>	SA7	I
D	IRQ3	>	B25	A25	<>	SA6	D
E	DACK2*	<	B26	A26	<>	SA5	E
	TC	<	B27	A27	<>	SA4	
	BALE	<	B28	A28	<>	SA3	
	+5 Volts	<	B29	A29	<>	SA2	
	OSC	<	B30	A30	<>	SA1	
	Ground	<	B31	A31	<>	SA0	

Notes:
Pin B4 is IRQ2 for an XT
Pin B4 is IRQ9 for an AT which is re-directed as IRQ2
A System Board Jumper on the original IBM AT provided the option of driving the clock (BCLK) signal from an adapter board device. Most clones do not support this option.
* = active low

3. ISA 36 Pin Connector

(this end nearest 62-pin connector)

	MEMCS16*	>	D1	C1	>	SBHE	
	I/OCS16*	>	D2	C2	<>	LA23	
	IRQ10	>	D3	C3	<>	LA22	
	IRQ11	>	D4	C4	<>	LA21	C
S	IRQ12	>	D5	C5	<>	LA20	O
O	IRQ15	>	D6	C6	<>	LA19	M
L	IRQ14	>	D7	C7	<>	LA18	P
D	DACK0*	<	D8	C8	<>	LA17	O
E	DRQ0	>	D9	C9	>	MEMR*	N
R	DACK5*	<	D10	C10	>	MEMW*	E
	DRQ5	>	D11	C11	<>	SD08	N
S	DACK6*	<	D12	C12	<>	SD09	T
I	DRQ6	>	D13	C13	<>	SD10	
D	DACK7*	<	D14	C14	<>	SD11	S
E	DRQ7	>	D15	C15	<>	SD12	I
	+5 Volts		D16	C16	<>	SD13	D
	MASTER16*	>	D17	C17	<>	SD14	E
	Ground		D18	C18	<>	SD15	

Symbols pointing toward the connector designate signals into the system board (from devices on the bus), and vice versa. <> indicates bi-directional signals.

NOTE: In the PC and PC/XT, the bus consists only of the 62-pin portion. Some of the signal names are different, but the functionality remains the same.

4. PC/104 Connector

Pin #	J1/P1 Row A	J1/P1 Row B	J2/P2 (1) Row C	J2/P2 (1) Row D
0			0V	0V
1	IOCHK*	0V	SBHE*	MEMCS16*
2	SD7	RESET	LA23	IOCS16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	-5V	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	-12V	LA18	IRQ14
8	SD1	SRDY	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	KEY (2)	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	MASTER*
18	SA13	DRQ1	SD15	0V
19	SA12	REFRESH*	KEY (2)	OV
20	SA11	BCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2*		
27	SA4	TC		
28	SA3	BALE		
29	SA2	+5V		
30	SA1	OSC		
31	SA0	0V		
32	OV	0V		

Notes: (1) Use Rows C and D for AT (16 bit).
(2) Keys are missing pins and filled holes.
* = active low

5. EISA Connector

Row F	Row B	Pin	Row E	Row A
GND	GND	1	CMD*	IOCHK*
+5V	RESET	2	START*	SD<7>
+5V	+5V	3	EXRDY	SD<6>
XXXXX	IRQ<9>	4	EX32*	SD<5>
XXXXX	-5V	5	GND	SD<4>
KEY	DRQ<2>	6	KEY	SD<3>
XXXXX	-12V	7	EX16*	SD<2>
XXXXX	SRDY*	8	SLBURST*	SD<1>
+12V	+12V	9	MSBURST*	SD<0>
M-IO	GND	10	W-R	IOCHRDY
LOCK*	SMEMW*	11	GND	AENx
RESERVED	SMEMR*	12	EMB66* (1)	SA<19>
GND	IOW*	13	EMB133* (1)	SA<18>
RESERVED	IOR*	14	RESERVED	SA<17>
BE*<3>	DACK*<3>	15	GND	SA<16>
KEY	DRQ<3>	16	KEY	SA<15>
BE*<2>	DACK*<1>	17	BE*<1>	SA<14>
BE*<0>	DRQ<1>	18	LA*<31>	SA<13>
GND	REFRESH*	19	GND	SA<12>
+5V	BCLK	20	LA*<30>	SA<11>
LA*<29>	IRQ<7>	21	LA*<28>	SA<10>
GND	IRQ<6>	22	LA*<27>	SA<9>
LA*<26>	IRQ<5>	23	LA*<25>	SA<8>
LA*<24>	IRQ<4>	24	GND	SA<7>
KEY	IRQ<3>	25	KEY	SA<6>
LA<16>	DACK*<2>	26	LA<15>	SA<5>
LA<14>	TC	27	LA<13>	SA<4>
+5V	BALE	28	LA<12>	SA<3>
+5V	+5V	29	LA<11>	SA<2>
GND	OSC	30	GND	SA<1>
LA<10>	GND	1	LA<9>	SA<0>

Row H	Row D		Row G	Row C
LA<8>	MEMCS16*	1	LA<7>	SBHE*
LA<6>	IOCS16*	2	GND	LA<23>
LA<5>	IRQ<10>	3	LA<4>	LA<22>
+5V	IRQ<11>	4	LA<3>	LA<21>
LA<2>	IRQ<12>	5	GND	LA<20>
KEY	IRQ<15>	6	KEY	LA<19>
DATA<16>	IRQ<14>	7	DATA<17>	LA<18>
DATA<18>	DACK*<0>	8	DATA<19>	LA<17>
GND	DRQ<0>	9	DATA<20>	MEMR*
DATA<21>	DACK*<5>	10	DATA<22>	MEMW*
DATA<23>	DRQ<5>	11	GND	SD<8>
DATA<24>	CACK*<6>	12	DATA<25>	SD<9>
GND	DRQ<6>	13	DATA<26>	SD<10>
DATA<27>	CACK*<7>	14	DATA<28>	SD<11>
KEY	DRQ<7>	15	KEY	SD<12>
DATA<29>	+5V	16	GND	SD<13>
+5V	MASTER16*	17	DATA>30>	SD>14?
+5V	GND	18	DATA<31>	SD<15>
MAKx*		19	MREQx*	

Order of reserved pin assignments: E12, E13, E14, F12, F14
XXXXX pins for manufacturer-specific use. Add-on cards must NOT CONNECT to these pins.
(1) E12 & E13 for Fast EISA, otherwise pull up thru 300 ohms.
* = active low

6. PCI Connectors

The following table is taken from the *PCI Handbook*, available from Annabooks.

	5V System		3.3V System	
Pin	Side B	Side A	Side B	Side A
32-Bit Connector Start				
1	-12V	TRST#	-12V	TRST#
2	TCK	+12V	TCK	+12V
3	GND	TMS	GND	TMS
4	TDO	TDI	TDO	TDI
5	+5V	+5V	+5V	+5V
6	+5V	INTA#	+5V	INTA#
7	INTB#	INTC#	INTB#	INTC#
8	INTD#	+5V	INTD#	+5V
9	PRSNT1#	RSVD	PRSNT1#	RSVD
10	RSVD	+5V (I/O)	RSVD	+3.3V (I/O)
11	PRSNT2#	RSVD	PRSNT2#	RSVD
12	GND	GND	KEY	KEY
13	GND	GND	KEY	KEY
14	RSVD	RSVD	RSVD	RSVD
15	GND	RST#	GND	RST#
16	CLK	+5V (I/O)	CLK	+3.3V (I/O)
17	GND	GNT#	GND	GNT#
18	REQ#	GND	REQ#	GND
19	+5V (I/O)	RSVD	+3.3V (I/O)	RSVD
20	AD[31]	AD[30]	AD[31]	AD[30]
21	AD[29]	+3.3V	AD[29]	+3.3V
22	GND	AD[28]	GND	AD[28]
23	AD[27]	AD[26]	AD[27]	AD[26]
24	AD[25]	GND	AD[25]	GND
25	+3.3V	AD[24]	+3.3V	AD[24]
26	C/BE[3]#	IDSEL	C/BE[3]#	IDSEL
27	AD[23]	+3.3V	AD[23]	+3.3V
28	GND	AD[22]	GND	AD[22]
29	AD[21]	AD[20]	AD[21]	AD[20]
30	AD[19]	GND	AD[19]	GND
31	+3.3V	AD[18]	+3.3V	AD[18]

6. PCI Connectors (cont.)

32	AD[17]	AD[16]	AD[17]	AD[16]
33	C/BE[2]#	+3.3V	C/BE[2]#	+3.3V
34	GND	FRAME#	GND	FRAME#
35	IRDY#	GND	IRDY#	GND
36	+3.3V	TRDY#	+3.3V	TRDY#
37	DEVSEL#	GND	DEVSEL#	GND
38	GND	STOP#	GND	STOP#
39	LOCK#	+3.3V	LOCK#	+3.3V
40	PERR#	SDONE	PERR#	SDONE
41	+3.3V	SBO#	+3.3V	SBO#
42	SERR#	GND	SERR#	GND
43	+3.3V	PAR	+3.3V	PAR
44	C/BE[1]#	AD[15]	C/BE[1]#	AD[15]
45	AD[14]	+3.3V	AD[14]	+3.3V
46	GND	AD[13]	GND	AD[13]
47	AD[12]	AD[11]	AD[12]	AD[11]
48	AD[10]	GND	AD[10]	GND
49	GND	AD[09]	GND	AD[09]
50	Key	Key	GND	GND
51	Key	Key	GND	GND
52	AD[08]	C/BE[0]#	AD[08]	C/BE[0]#
53	AD[07]	+3.3V	AD[07]	+3.3V
54	+3.3V	AD[06]	+3.3V	AD[06]
55	AD[05]	AD[04]	AD[05]	AD[04]
56	AD[03]	GND	AD[03]	GND
57	GND	AD[02]	GND	AD[02]
58	AD[01]	AD[00]	AD[01]	AD[00]
59	+5V (I/O)	+5V (I/O)	+3.3V (I/O)	+3.3V (I/O)
60	ACK64#	REQ64#	ACK64#	REQ64#
61	+5V	+5V	+5V	+5V
62	+5V	+5V	+5V	+5V
32-Bit Connector End				
	Key	Key	Key	Key
	Key	Key	Key	Key
64-Bit Connector Start				
63	RSVD	GND	RSVD	GND
64	GND	C/BE[7]#	GND	C/BE[7]#
65	C/BE[6]#	C/BE[5]#	C/BE[6]#	C/BE[5]#
66	C/BE[4]#	+5V (I/O)	C/BE[4]#	+3.3V (I/O)

6. PCI Connectors (cont.)

67	GND	PAR64	GND	PAR64
68	AD[63]	AD[62]	AD[63]	AD[62]
69	AD[61]	GND	AD[61]	GND
70	+5V (I/O)	AD[60]	+3.3V (I/O)	AD[60]
71	AD[59]	AD[58]	AD[59]	AD[58]
72	AD[57]	GND	AD[57]	GND
73	GND	AD[56]	GND	AD[56]
74	AD[55]	AD[54]	AD[55]	AD[54]
75	AD[53]	+5V (I/O)	AD[53]	+3.3V (I/O)
76	GND	AD[52]	GND	AD[52]
77	AD[51]	AD[50]	AD[51]	AD[50]
78	AD[49]	GND	AD[49]	GND
79	+5V (I/O)	AD[48]	+3.3V (I/O)	AD[48]
80	AD[47]	AD[46]	AD[47]	AD[46]
81	AD[45]	GND	AD[45]	GND
82	GND	AD[44]	GND	AD[44]
83	AD[43]	AD[42]	AD[43]	AD[42]
84	AD[41]	+5V (I/O)	AD[41]	+3.3V (I/O)
85	GND	AD[40]	GND	AD[40]
86	AD[39]	AD[38]	AD[39]	AD[38]
87	AD[37]	GND	AD[37]	GND
88	+5V (I/O)	AD[36]	+3.3V (I/O)	AD[36]
89	AD[35]	AD[34]	AD[35]	AD[34]
90	AD[33]	GND	AD[33]	GND
91	GND	AD[32]	GND	AD[32]
92	RSVD	RSVD	RSVD	RSVD
93	RSVD	GND	RSVD	GND
94	GND	RSVD	GND	RSVD
64-Bit Connector End				

NOTE:

1. Pins marked "+5V (I/O)" or "+3.3V (I/O)" on the system board are connected to "V (I/O)" (3.3V or 5V) on the expansion (universal) board.

= active low

7. Small PCI (SPCI) Connector

Pin	Side B	Side A	Pin	Side B	Side A
1	GND	GND	28	AD[17]	AD[16]
2	INTB#	+12V	29	C/BE[2]#	+3.3V
3	+5V	INTA#	30	GND	FRAME#
4	INTD#	INTC#	31	IRDY#	GND
5	-12V	+5V	32	+3.3V	TRDY#
6	PRSNT1#	Reserved	33	DEVSEL#	GND
7	Reserved	Reserved	34	GND	STOP#
8	PRSNT2#	+5V	35	LOCK#	+3.3V
9	CLK	RST#	36	PERR#	SDONE
10	GND	GNT#	37	GND	SB0#
11	REQ#	GND	38	SERR#	GND
12	+5V	CLKRUN#	39	+3.3V	PAR
13	AD[31]	AD[30]	40	C/BE[1]#	AD[15]
14	AD[29]	+5V	41	AD[14]	+3.3V
15	GND	AD[28]	42	GND	AD[13]
16	AD[27]	AD[26]	43	AD[12]	AD[11]
17	AD[25]	GND	44	AD[10]	M66EN
18	+Vi/o	AD[24]	45	+Vi/o	AD[09]
19	Reserved	+Vi/o	46	AD[08]	C/BE[0]#
20	GND	Reserved	47	AD[07]	+Vi/o
21	C/BE[3]#	GND	48	+5V	AD[06]
22	+3.3V	IDSEL	49	AD[05]	AD[04]
23	AD[23]	+3.3V	50	AD[03]	+5V
24	GND	AD[22]	51	+5V	AD[02]
25	AD[21]	AD[20]	52	AD[01]	AD[00]
26	AD[19]	GND	53	ACK64#	GND
27	+3.3V	AD[18]	54	GND	REQ64#

PRSNT1#	PRSNT2#	PCI	SMALL PCI
Open	Open	No board present	No board present
Ground	Open	25W maximum	10W maximum
Open	Ground	15W maximum	5W maximum
Ground	Ground	7.5W maximum	2W maximum

8. SPCI Recommended I/O Pinouts

Ethernet (10BASE-T and AUI)

Pin	Description
1	10BASE-T Receive, Negative Phase
2	12BASE-T Receive, Positive Phase
3	Receive LED
4	AUI Receive, Negative Phase
5	AUI Receive, Positive Phase
6	10BASE-T Link Status LED
7	Cable Activity (transmit) LED
8	AUI Transmit, Negative Phase
9	AUI Transmit, Positive Phase
10	Power out of PC card to external modules (+12V)
11	AUI Collision Input, Negative Phase
12	AUI Collision Input, Positive Phase
13	Ground
14	10BASE-T Transmit, Negative Phase
15	10BASE-T Transmit, Positive Phase

Token Ring (STP or UTP)

Pin	Description
1	Transmit Negative Phase
2	Transmit Positive Phase
3	Power into PC card from external supply
4	STP Receive, Negative Phase
5	STP Receive, Positive Phase
6	Transmit Status LED
7	Receive Status LED
8	not connected
9	not connected
10	Power out of PC card to external modules
11	UTP Receive, Negative Phase
12	UTP Receive, Positive Phase
13	Ground
14	STP Transmit, Negative Phase
15	STP Transmit, Positive Phase

8. SPCI Recommended I/O Pinouts (cont.)

Single-Ended 8-Bit SCSI

Pin	Description	Pin	Description
1	D0	18	GND
2	GND	19	TERMPWR
3	D1	20	TERMPWR
4	GND	21	ATN
5	D2	22	BSY
6	GND	23	RST
7	D3	24	GND
8	GND	25	MSG
9	D4	26	SEL
10	GND	27	C/D
11	D5	28	I/O
12	GND	29	GND
13	D6	30	REQ
14	GND	31	not connected
15	D7	32	GND
16	GND	33	ACK
17	DP		

VGA/SVGA

Pin	Description
1	Red Video
2	Green Video
3	Blue Video
4	Monitor ID Bit 2
5	Ground
6	Red Return
7	Green Return
8	Blue Return
9	No Connection
10	Sync Return
11	Monitor ID Bit 0
12	Monitor ID Bit 1
13	Horizontal Sync
14	Vertical Sync
15	Monitor ID Bit 3

9. VESA VL Bus Connector

Row B, 64 bit	Row B, 32 bit	Pin	Row A, 32 bit	Row A, 64 bit
	D0	1	D1	
	D2	2	D3	
	D4	3	GND	
	D6	4	D5	
	D8	5	D7	
	GND	6	D9	
	D10	7	D11	
	D12	8	D13	
	Vcc	9	D15	
	D14	10	GND	
	D16	11	D17	
	D18	12	Vcc	
	D20	13	D19	
	GND	14	D21	
	D22	15	D23	
	D24	16	D25	
	D26	17	GND	
	D28	18	D27	
	D30	19	D29	
	Vcc	20	D31	
D63	A31	21	A30	D62
	GND	22	A28	D60
D61	A29	23	A26	D58
D59	A27	24	GND	
D57	A25	25	A24	D56
D55	A23	26	A22	D54
D53	A21	27	Vcc	
D51	A19	28	A20	D52
	GND	29	A18	D50
D49	A17	30	A16	D48
D47	A15	31	A14	D46
	Vcc	32	A12	D44
D45	A13	33	A10	D42
D43	A11	34	A8	D40
D41	A9	35	GND	
D39	A7	36	A6	D38
D37	A5	37	A4	D36
	GND	38	WBACK*	
D35	A3	39	BE0*	BE4*
D34	A2	40	Vcc	
LBS64*	free	41	BE1*	BE5*
	RESET*	42	BE2*	BE6*
	D/C*	43	GND	
D33	M/IO*	44	BE3*	BE7*
D32	W/R*	45	ADS*	
	RDYRTN*	48	LRDY*	
	GND	49	LDEV<x>*	
	IRQ9	50	LREQ<x>	
	BRDY*	51	GND	
	BLAST	52	LGNT<x>	
	ID0	53	Vcc	
	ID1	54	ID2	
	GND	55	ID3	
	LCLK	56	ID4	ACK64*
	Vcc	57	LKEN*	
	LBS16*	58	LEADS*	

The 64 bit signals are multiplexed with the shared 32 bit pins.
* = active low

10. PC Card (PCMCIA) Connector

Mem and I/O	Mem only	Pin	Pin	Mem only	Mem and I/O
	GND	35	1	GND	
	CD1*	36	2	D3	
	D11	37	3	D4	
	D12	38	4	D5	
	D13	39	5	D6	
	D14	40	6	D7	
	D15	41	7	CE1*	
	CD2*	42	8	A10	
	RFSH	43	9	OE*	
IORD*	reserved	44	10	A11	
IOWR*	reserved	45	11	A9	
	A17	46	12	A8	
	A18	47	13	A13	
	A19	48	14	A14	
	A20	49	15	WE*/PGM*	
	A21	50	16	RDY/BSY*	IREQ*
	Vcc	51	17	Vcc	
	Vpp2	52	18	Vpp1	
	A22	53	19	A16	
	A23	54	20	A15	
	A24	55	21	A12	
	A25	56	22	A7	
	reserved	57	23	A6	
	RESET	58	24	A5	
	WAIT*	59	25	A4	
INPACK*	reserved	60	26	A3	
	REG*	61	27	A2	
SPKR*	BVD2	62	28	A1	
STSCHG*	BVD1	63	29	A0	
	D8	64	30	D0	
	D9	65	31	D1	
	D10	66	32	D2	
	CD2*	67	33	WP	IOIS16*
	GND	68	34	GND	

* = active low
low numbered pins are on top of card

11. ISA Signal Names

The signal line names have varied between the documentation of the original PC, the XT, AT, the ISA specification, the EISA specification, the PC/104 specification and between different manufacturers. The following list are the names used in Ed Solari's "ISA & EISA Theory and Operation" (Annabooks). The majority of names match those in the EISA Rev. 3.12 specification. The names listed avoid the use of "-" and "/" to denote an active low signal, using the * as in the EISA specification. Other versions of the signal names are shown in parentheses. Pin number (ISA and EISA connector) is the first of a series.

AENx		A11
BALE	(ALE)	B28
BCLK	(CLK)	B20
BE*		F18
CMD*		E1
DACKx*	(DACK*, DAKx*)	B8
DRQx		B9
EX16*		E7
EX32*		E4
EXRDY		E3
IOCHK*	(IOCHCK*, I/OCHCK*)	A1
IOCHRDY	(CHRDY, I/OCHRDY)	A10
IOCS16*	(IO16*, I/OCS16*)	D2
IOR*	(IORC*)	B14
IOW*	(IOWC*)	B13
IRQx		B25
LA* & LA		F5
LOCK*		F11
M-IO	(M-I/O)	F10
MAKx*	(MACKx*)	H19
MASTER16*	(MASTER)	D17
MEMCS16*	(M16*)	D1
MEMR*	(MRDC*)	A9
MEMW*	(MWTC*)	A10
MREQx*		E19
MSBURST*	(MBURST*)	E9
OSC		B30
REFRESH*	(REF*, old DACK<0>)	B19
RESET	[RESDRV, RESETDRV)	B2
SA	(A)	A31
SBHE*		C1
SD	(D, DATA)	A9
SLBURST*	(SBURST*)	E8
SMEMR*	(SMRDC*)	B12
SMEMW*	(SMWTC*)	B11
SRDY*	(NOWS*, 0WS*, ENDXFR)	B8
START*		E2
TC	(T-C, T/C)	B27
W-R	(W/R)	E10

12. ISA Bus Signal Summary

Since the XT and AT (ISA) buses are subsets of the EISA bus, this section has been changed to use the EISA set of signal names described in the preceeding section. Please also see the preceeding section for some of the alternative or older names for some of the lines. The descriptions below are brief by necessity; designers should refer to other sources, such as "ISA & EISA Theory and Operation" (Annabooks) for more details.

Name	Description
AENx	Address Enable. Indicates DMA controller is bus master (ISA). Also used by EISA for slot-specific I/O addressing (x = slot number).
BALE	Bus Latch Enable. Indicates that SA, LA, AENx, and SBHE* signal lines are valid.
BCLK	Bus Clock. 4.77 MHz 33% duty cycle on PC and XT. 50% duty cycle 6 MHz for AT, and 8 or 8.33 MHz for EISA. 4.0 MHz minimum for EISA.
BE*<0-3>	Byte Enable. Indicates which byte lanes are valid. EISA only.
CMD*	Command. Controls cycle timing after active START* signal. EISA only.
DACKx*	DMA Acknowledge. Used by DMA controller to select an I/O resource that requested the bus (DRQx). Used by ISA bus master to gain control of the bus from DMA controller. DACK<0> used by XT and AT computers for memory refresh.
DRQx	DMA Request. Used by I/O resources to request DMA service. Must be held high until associated DACKx* line is active.
EX16* EX32*	EISA Access 16 or 32 data bit. Indicates data width of an EISA resource. Also driven by platform circuitry to indicate completion of certain cycles.
EXRDY	EISA Access Ready. Driven by EISA resource to indicate additional cycle time is required.
IOCHK*	I/O Channel Check. Driven by any resource to indicate a bus error, such as parity. Only serviced by platform circuitry. Usually sends NMI to CPU.

12. ISA Bus Signal Summary (cont.)

IOCHRDY	I/O Channel Ready. Driven inactive by a bus resource that needs additional cycles. Must not be held inactive for more than 15.6 usec or refresh may be missed.
IOCS16*	I/O Chip Select 16. Indicates that a resource supports 16 bit accesses. Ignored by DMA and refresh controllers.
IOR* IOW*	I/O Read (Write). Used by ISA & EISA bus master or DMA controller to request non-EISA I/O resource to drive data (or read data) on data lines. Not defined for EISA bus master and EISA I/O resources. (See M-IO and W-R.)
IRQx	Interrupt Request. Used by add-on card to request service by platform. Edge-triggered (ISA) allows one card per line. Level triggered option (EISA) allows sharing.
LA<2-16>	Latchable Address. LA<2-16> (EISA only) are latchable address lines. Must be latched by the resource if they are required for the entire cycle. See SA for ISA.
LA<17-23>	Same, except they appear on the 16 bit part of the ISA connector.
LA*<24-31>	Highest byte of the 32 bit (EISA) latchable address bus. Same function as LA except for inverted logic.
LOCK*	Lock. Insures exclusive memory or I/O access by the EISA bus master that drives it active. Cannot be used during DMA transfer cycles or during certain other cycles.
M-IO	Memory-I/O. Defines memory cycle (high) or I/O cycle (low). EISA only.
MAKx*	Master Acknowledge. Used by EISA platform arbiter to award bus master in response to a request (see MREQx*). EISA only.
MASTER16*	Master 16 bit. Used by add-on bus master to indicate 16 bit data size. With EISA platform and add-on bus master, non-assertion indicates 32 bit bus master.

12. ISA Bus Signal Summary (cont.)

MEMCS16* Memory Chip Select 16. Driven by memory resource to indicate support of 16 bit accesses. Also allows bus master to execute shorter cycles. Bus master must ignore this line during I/O access cycles. Also ignored by DMA and refresh controllers. Not defined when EISA bus master accessing EISA resource.

MEMR* Memory Read (Write). Used by the bus owner to
MEMW* request a memory resource to drive (accept) data. See also SMEMR* and SMEMW*.

MREQx* Master Request. Used by EISA add-on card (in slot x) to request bus ownership. See also MAKx.

MSBURST* Master Burst. Used by EISA bus owner to notify accessed resource that it will execute a burst access cycle. Burst access cycle occurs only if both MSBURST* and SLBURST* are active.

NOWS* See SRDY*.

OSC Oscillator. A 50% duty cycle clock at 14.31818 MHz. Used originally for color burst in composite video. Not synchronized to any other signal.

REFRESH* Memory Refresh. Indicates a refresh cycle is in progress. Memory is refreshed every 15.6 usec.

RESET Used to reset or initialize system logic on power up, during low line voltage, or after a bus timeout. EISA systems allow software to issue reset by setting bit 0 of I/O port 0461h to a "1". Setting the bit to a "0" negates command.

SA System Address. Address lines for the first one megabyte of memory. SA<0-9> used for I/O addresses. SA<0> is the least significant bit.

SBHE* System Byte High Enable. Indicates valid data on SD<8-15> lines. Inactive indicates 8 bit data width. Not used when EISA bus master accesses EISA resources.

SD System Data. SD<0> is the least significant bit. Platform byte swapper circuitry assures SD<8-15> valid when SBHE* is active.

12. ISA Bus Signal Summary (cont.)

SLBURST* Slave Burst. An EISA slave asserts this line to indicate that it can support a burst access cycle. See also MSBURST*.

SMEMR* System Memory Read (Write). Requests a
SMEMW* memory resource to drive (accept) data. Purpose is to maintain compatiblilty with 8 bit add-on cards. Derived from MEMR* (or MEMW*) and LA<20-23>, so timing lags.

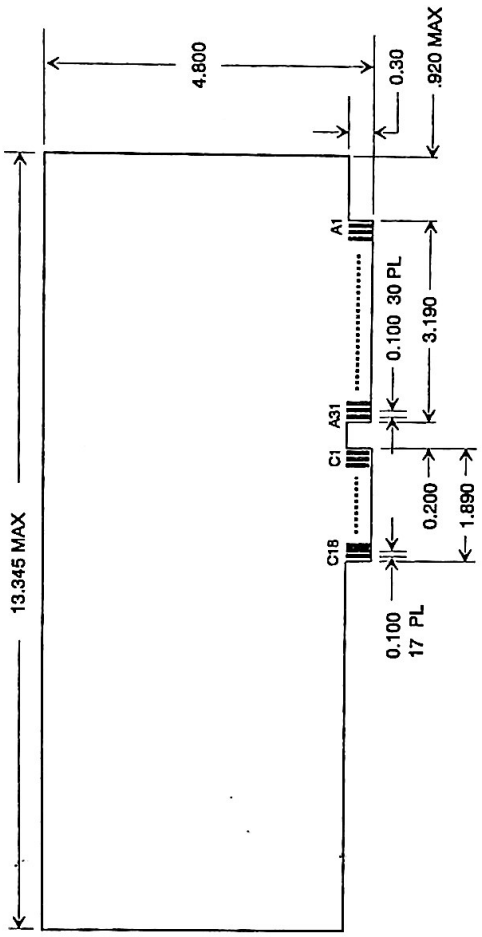
SRDY* Synchronous Ready (NO Wait State). Asserted by
(NOWS*) accessed resource to indicate that a shorter access cycle can be executed.

START* Indicates the beginning of an EISA access cycle and the initial qualification of other signal lines.

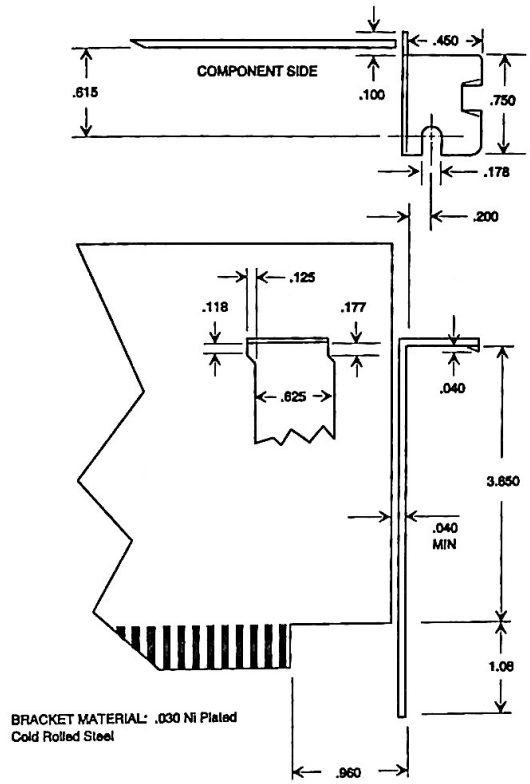
TC Terminal Count. Driven by the DMA contoller to indicate completion of data transfer. Can be bi-directional for EISA.

W-R Write (high) - Read (low). Indicates to accessed resource whether to accept data or drive data. May be driven by the bus master, refresh controller, DMA controller, or platform circuitry depending on the cycle. EISA only.

13. AT Add-On Card Dimensions



14. Card Bracket Position

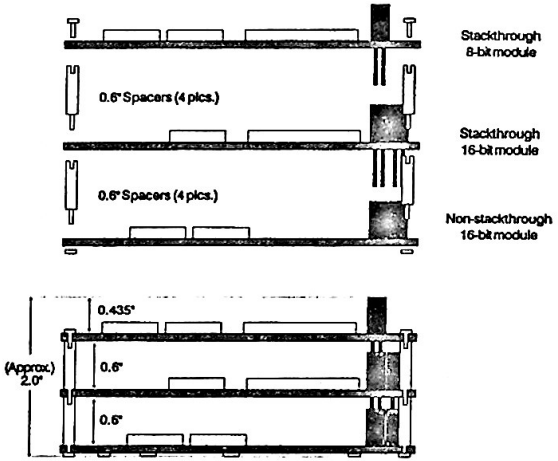


(The .960 shown was .990 in the original IBM PC, but has changed over the years; .960 is a better fit in most chassis.)

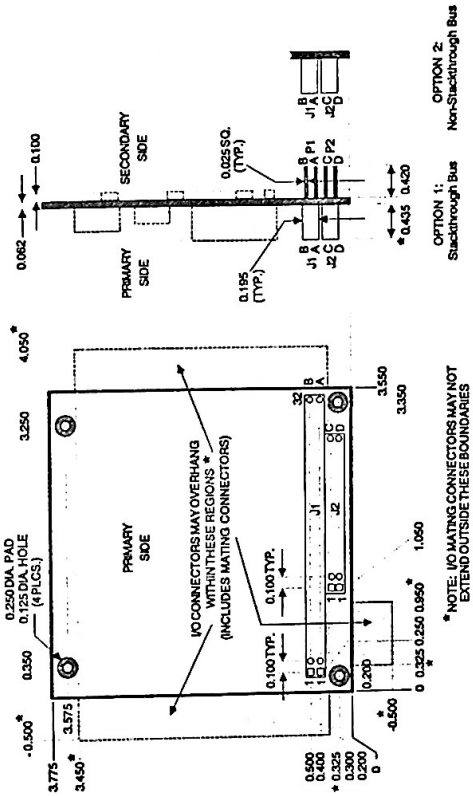
15. PC/104 Cards

The PC/104 bus has the same electrical specifications (with one exception noted below) as the ISA bus. PC/104 provides a more compact form factor, and reduced drive requirements on most lines. This page shows the stacking of the various types of modules, and the next page shows the dimensions for the 16-bit (AT) module. J2 and P2 may be eliminated for an 8-bit (XT) module. MEMCS16*, IOCS16*, MASTER*, and ENDXFR* (SRDY) must be driven with devices capable of providing 20 mA sink current. All others need sink only 4 mA.

PC/104 is a trademark of the PC/104 Consortium. The following drawings (Copyright 1992-94, PC/104 Consortium) are reprinted with permission. To obtain copies of the PC/104 specification, please contact PC/104, 809 Cuesta Drive, B-175, Mt. View, CA 94040, 415-903-8304.



Typical Module Stack



PC/104 16-Bit Module Dimensions

16. Power Cables

PS-8
Connector: 6 pin Molex

1	Pwr Good
2	+5v
3	+12v
4	-12v
5	gnd
6	gnd

PS-9
Connector: 6-pin Molex

1	gnd	gnd
2	gnd	gnd
3	-5v	-5v
4	+5v	+5v
5	+5v	+5v
6	+5v	+5v

Disk drive power
Connector: 4-pin Molex

1	+12v
2	gnd
3	gnd
4	+5v

AT Battery connector
Connector: 4-pin Berg

1	gnd
2	unused
3	key
4	+6v

AT LED and Keylock connector
Connector: 5-pin Berg

1	LED Power (+5v)
2	key
3	Gnd
4	Keyboard inhibit
5	Gnd

17. Display Cables

MDA (Hercules) Display:
Connector: Female 9-Pin D-Sub, cable requires male.

Pin	I/O	Description
1		Ground
2		Ground
3		Not Used
4		Not Used
5		Not Used
6	>	+Intensity
7	>	+Video
8	>	+Horizontal
9	>	-Vertical

CGA Display:
Connector: Female 9-Pin D-Sub, cable requires male.

Pin	I/O	Description
1		Ground
2		Ground
3	>	Red
4	>	Green
5	>	Blue
6	>	Intensity
7	>	Reserved
8	>	Horizontal Drive
9	>	Vertical Drive

EGA RGB Display:
Connector: Female 9-Pin D-Sub, cable requires male.

Pin	I/O	Description
1		Ground
2	>	S. red
3	>	Red
4	>	Green
5	>	Blue
6	>	S. green/Intensity
7	>	S. blue/mono video
8	>	Horizontal Drive
9	>	Vertical Drive

17. Display Cables (cont.)

VGA RGB Display:

Connector: Female 15-Pin D-Sub, cable requires male.

Pin	I/O	Descr.	Mono Use	Color Use
1	>	Red		Red
2	>	Green	Mono	Green
3	>	Blue		Blue
4		reserved		
5		Digital Gnd	Self Test	Self Test
6	<	Red return	Key	R. return
7	<	Grn return	Mono return	G. return
8	<	Blue return		B. return
9		Plug		
10		Digital Gnd	Gnd	Gnd
11		reserved		Gnd
12		reserved		Gnd
13	>	H. Drive	H. Drive	H. Drive
14	>	V. Drive	V. Drive	V. Drive
15		reserved		

CGA Composite Video:

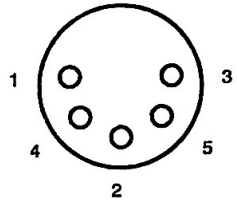
Connector: RCA phono jack, cable requires male

Pin	I/O	Description
1	<	(Pin) 1.5Vdc Composite video
2	<	(Shell) Ground

18. Keyboard Cable

Connector: 5-Pin DIN Female, cable requires male.

Pin	Name
1	+Keyboard Clock
2	+Keyboard Data
3	-Keyboard Reset
4	Ground
5	+5 Volts

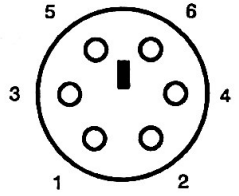


Cable (male) pinout

18. Keyboard Cable (cont.)

Connector: 6-Pin Miniature DIN Female, cable requires male. Used for laptops and PS/1 & 2 keyboard and mouse.

Pin	Name
1	+Keyboard Data
2	Unused
3	Ground
4	+5 Volts
5	Clock
6	Unused



Cable (male) pinout

19. Parallel Printer Cable

PC (D-25 male) --**Prn** (Amphenol 57-30360 male)

Description	PC-Pin	Direct.	Prn-Pin
-Strobe	1	<>	1
+Data Bit 0	2	<>	2
+Data Bit 1	3	<>	3
+Data Bit 2	4	<>	4
+Data Bit 3	5	<>	5
+Data Bit 4	6	<>	6
+Data Bit 5	7	<>	7
+Data Bit 6	8	<>	8
+Data Bit 7	9	<>	9
-Acknowledge	10	<	10
+Busy	11	<	11
+Paper End	12	<	12
+Select	13	<	13
-Auto Feed	14	>	14
-Error/Fault	15	<	32
-Printer Init	16	>	31
-Select	17	>	36
Ground	18-25		19-30
-Printer Init	16	>	31
-Error/Fault	15	<	32
Ground			33
Not Used			34
+5v through 4.7K			35
-Select	17	<	36

20. RS-232C Cables

Serial Adapter Connector: Male 25-Pin D-Sub
Unlisted pins have no connection.

Pin	I/O	Description
1		NC (Shield Gnd. Other End)
2	>	TX (Transmit Data)
3	<	RX (Receive Data)
4	>	RTS (Request to Send)
5	<	CTS (Clear to Send)
6	<	DSR (Data Set Ready)
7		GND (Signal Ground)
8	<	DCD (Data Carrier Detect)
9	>	+Transmit Current Loop Data
11	>	-Transmit Current Loop Data
18	<	+Receive Current Loop Data
20	>	DTR (Data Terminal Ready)
22	<	RI (Ring Indicator)
25	<	-Receive Current Loop Data

Alternate Adapter Connector: Male 9-Pin D-Sub

Pin	I/O	Description
1	<	DCD (Data Carrier Detect)
2	<	RX (Receive Data)
3	>	TX (Transmit Data)
4	>	DTR (Data Terminal Ready)
5		GND (Signal Ground)
6	<	DSR (Data Set Ready)
7	>	RTS (Request To Send)
8	<	CTS (Clear To Send)
9	<	RI (Ring Indicator)

To wire a 25-pin connector to a 9-pin connector:

DB-9	DB-25	Description
1	8	DCD (Data Carrier Detect)
2	3	RX (Receive Data)
3	2	TX (Transmit Data)
4	20	DTR (Data Terminal Ready)
5	7	GND (Signal Ground)
6	6	DSR (Data Set Ready)
7	4	RTS (Request To Send)
8	5	CTS (Clear To Send)
9	22	RI (Ring Indicator)

21. Null Modem Cable

To connect two computers' serial ports together, or other devices that may consider themselves Data Sources, use the following connnections to make a null modem cable.
Unlisted pins have no connection.

25-Pin D-Sub

System 1	Pin	Pin	System 2
TX	2	3	RX
RX	3	2	TX
RTS	4	8	DCD
CTS	5		
DSR	6	20	DTR
DCD	8	4	RTS
		5	CTS
DTR	20	6	DSR

Pins 4 and 5 are shorted together on each connector.

9-Pin D-Sub

System 1	Pin	Pin	System 2
TX	3	2	RX
RX	2	3	TX
RTS	7	1	DCD
CTS	8		
DSR	6	4	DTR
DCD	1	7	RTS
		8	CTS
DTR	4	6	DSR

Pins 7 and 8 are shorted together on each connector.

22. Game Controller Adapter Cable

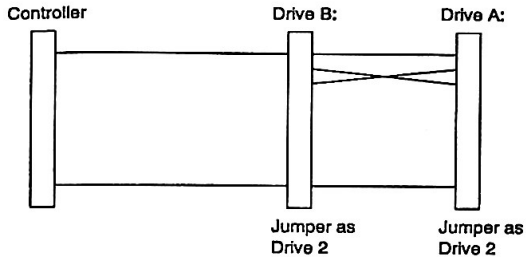
Connector: Female 15-Pin D-Sub, cable requires male.

Pin	I/O	Description
1	>	+5 Volts
2	<	Button 4
3	<	Position 0
4		Ground
5		Ground
6	<	Position 1
7	<	Button 5
8	>	+5 Volts
9	>	+5 Volts
10	<	Button 6
11	<	Position 2
12		Ground
13	<	Position 3
14	<	Button 7
15	>	+5 Volts

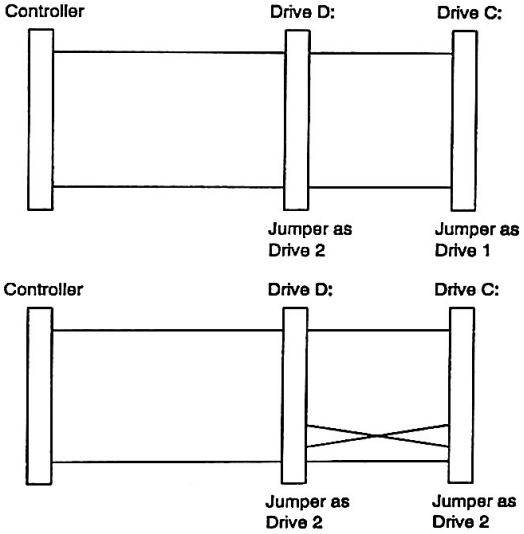
23. Disk Cables

The 34-conducter Disk Cables have three variations. The types and applicability of each is shown below:

Floppy Drives



Hard Drives



24. Disk Controller Function Summary

Information on this and following pages extracted from "Hard Drive Handbook" by Alting-Mees (coming soon from Annabooks).

ST506

All host interface circuitry located on expansion card.

Host to controller communications through Command Description Blocks (Task Descriptor Files or Task Files).

Host interface contoller connected to drive controller via 34-pin control cable and 20-pin data cable.

MFM data sent from host interface controller to drive controller.

ESDI

Data separator circuit located on drive electronics, all other interface electronics located on expansion card.

Host to controller communications through Command Description Blocks.

Host interface controller connected to drive controller via 34-pin control cable and 20-pin data cable.

NRZ data sent from host interface controller to drive controller.

SCSI

All controller functions and circuitry located on drive.

Host adapter (rather than interface controller) required to interface SCSI bus to PC bus.

Host to controller communications through Command Description Blocks.

Host (or adapter) SCSI software driver must translate from sectors (DOS) to data blocks.

IDE

All controller functions and circuitry located on drive.

Host to controller communications through Command Description Blocks.

Host computer or IDE adapter board connected to drive via 40-pin cable.

25. ST506 & ESDI Cables

34 Conductor Control Cable

Signal Name	Direction	Signal Pin #	Gnd Pin #
Reserved (sometimes Reduced WC Flag)	N/A	2	1
Head Select 2	>	4	3
Write Gate	>	6	5
Seek Complete	<	8	7
Track 0	<	10	9
Write Fault	<	12	11
Head Select 0*	>	14	13
Sector/Address Mark Found	<	16	15
Head Select 1	>	18	17
Index	<	20	19
Ready	<	22	21
Step	>	24	23
Drive Select 1	>	26	25
Drive Select 2	>	28	27
Drive Select 3	>	30	29
Drive Select 4	>	32	31
Direction	>	34	33

20 Conductor Data Cable

Drive Selected	<	1	2
Reserved	N/A	3	4
Reserved	N/A	5	6
**	N/A	7	8
Reserved	N/A	9	
Reserved	N/A	10	11
+ Write Data	>	13	12
- Write Data	>	14	15
+ Read Data	<	17	16
- Read Data	<	18	19, 20

* = Looped to pin 7 of data connector on the disk
** = Connected to pin 16 of the controller connector on the disk
> = From controller to disk
< = From disk to controller

34-pin connector: AMP 842-807-2005-007 or 3M 3461-0001
20-pin connector: AMP 842-807-3405-007 or 3M 3463-0001

26. ST506 & ESDI Signals

All signals active high.

Direction Set TRUE when moving heads towards center tracks, set FALSE when moving heads towards outer tracks.

Drive Select Used by the host to specify drive it wishes to access. On most drives, these lines serve only to gate other interface signals into the drive electronics (from the controller), or vice versa.

Head Select Three signals used to specify one of eight heads for upcoming read or write operation.

Index FALSE to TRUE edge. Signals the index mark has just passed under the head; this occurs once each revolution, or 16.67 ms for 3600 rpm.

Ready Set TRUE when drive speed and DC power are ready and Track 000 has been set TRUE.

Seek Complete SET TRUE when actuator has moved heads the required step distance. Set FALSE during power on.

Step Active pulse causes stepper motor to move the heads one track position in the direction indicated by the Direction line.

Track 000 TRUE during power on and when moving the heads from track 001 to 000.

Write Gate Set TRUE during write operations, FALSE during read operations.

Write Fault Set TRUE if an error has occurred during the operation. Errors include:
- Write current in head without Write Gate true
- No write current in head with Write Gate and Drive Select true
- Write Gate true, heads off-track and drive selected
- DC power out of tolerance

Drive Selected Set TRUE by the drive to acknowledge that its address matches the Drive Select.

Write Data Differential data lines that send data to the drive (MFM for ST506, NRZ for ESDI).

Read Data Differential data lines that read data from the drive (MFM for ST506, NRZ for ESDI).

27. SCSI Cables

The 50-pin SCSI "A" cable carries 8 data bits, one parity bit (odd), nine control lines, 30 ground lines, and one line to supply power to the terminators. Pin 25 is not connected in order to safeguard against accidental shorting of the termination power. The Reserved lines (open) must be connected to ground in the terminators.

Signal Name	Pin (Note 1)	Pin (Note 1)	Signal Name	Differential Cable Pins (Notes 1 & 2)
Shield Gnd				1 (1)
DB0*	2 (26)	1 (1)	GND	3, 4 (2, 27)
DB1*	4 (27)	3 (2)	GND	5, 6 (3, 28)
DB2*	6 (28)	5 (3)	GND	7, 8 (4, 29)
DB3*	8 (29)	7 (4)	GND	9, 10 (5, 30)
DB4*	10 (30)	9 (5)	GND	11, 12 (6, 31)
DB5*	12 (31)	11 (6)	GND	13, 14 (7, 32)
DB6*	14 (32)	13 (7)	GND	15, 16 (8, 33)
DB7*	16 (33)	15 (8)	GND	17, 18 (9, 34)
DBP	18 (34)	17 (9)	GND	19, 20 (10, 35)
GND	20 (35)	19 (10)	GND	22 (36)
GND	22 (36)	21 (11)	GND	
Reserved	24 (37)	23 (12)	Reserved	23, 24 (12 ,37)
TRMPWR	26 (38)	25 (13)	OPEN	25, 26 (13, 38)
Reserved	28 (39)	27 (14)	Reserved	27, 28 (14, 39)
GND	30 (40)	29 (15)	GND	
ATN*	32 (41)	31 (16)	GND	29, 30 (15, 40)
GND	34 (42)	33 (17)	GND	31, 32 (16, 41)
BSY*	36 (43)	35 (18)	GND	33, 34 (17, 42)
ACK*	38 (44)	37 (19)	GND	35, 36 (18, 43)
RST*	40 (45)	39 (20)	GND	37, 38 (19, 44)
MSG*	42 (46)	41 (21)	GND	39, 40 (20, 45)
SEL*	44 (47)	43 (22)	GND	41, 42 (21, 46)
C/D*	46 (48)	45 (23)	GND	43, 44 (22, 47)
REQ*	48 (49)	47 (24)	GND	45, 46 (23, 48)
I/O*	50 (50)	49 (25)	GND	47, 48 (24, 49)
GND				2, 49, 50 (25, 26, 50)
DIFFSENS				21 (11)

* = Active low
Note (1): Pins in ( ) are for "D" Style connector
Note (2): The first pin number is the inverse signal (e.g., DB0 is on pin 3 and DB0* is on pin 4)

External terminators: AMP 88-4163-081-1 or
DATA MATE DM500-06-8

Cable: 50 wire flat 28 AWG, 3M 3365-50 or equivalent.

27. SCSI Cable (cont.)

The 68-pin SCSI "B" cable carries data bits 8 through 31. There is also a 68-pin proposed "P" cable for use with 16 bits instead of using the "A" and "B" cables. The Reserved lines (open) must be connected to ground in the terminators.

Signal Name (Note 1)	Pin	Pin	Signal Name	Signal "P" Cable (Note 2)
	1	35	GND	DB12*
GND/DB8	2	36	DB8*	DB13*
GND/DB9	3	37	DB9*	DB14*
GND/DB10	4	38	DB10*	DB15*
GND/DB11	5	39	DB11*	DBP1*
GND/DB12	6	40	DB12*	GND
GND/DB13	7	41	DB13*	DB0*
GND/DB14	8	42	DB14*	DB1*
GND/DB15	9	43	DB15*	DB2*
GND/DBP1	10	44	DBP1*	DB3*
GND/ACKB	11	45	ACKB*	DB4*
GND	12	46	GND	DB4*
GND/REQB	13	47	REQB*	DB6*
GND/DB16	14	48	DB16*	DB7*
GND/DB17	15	49	DB17*	DBP*
GND/DB18	16	50	DB18*	GND
TERMPWRB	17	51	TERMPWRB	TERMPWRB
TERMPWRB	18	52	TERMPWRB	TERMPWRB
GND/DB19	19	53	DB19*	Reserved
GND/DB20	20	54	DB20*	ATN*
GND/DB21	21	55	DB21*	GND*
GND/DB22	22	56	DB22*	BSY*
GND/DB23	23	57	DB23*	ACK*
GND/DBP2	24	58	DBP2*	RST*
GND/DB24	25	59	DB24*	MSG*
GND/DB25	26	60	DB25*	SEL*
GND/DB26	27	61	DB26*	C/D*
GND/DB27	28	62	DB27*	REQ*
GND/DB28	29	63	DB28*	I/O*
GND/DB29	30	64	DB29*	GND
GND/DB30	31	65	DB30*	DB8*
GND/DB31	32	66	DB31*	DB9*
GND/DBP3	33	67	DBP3*	DB10*
GND	34	68	GND	DB11*

Note 1: Single ended/differential cable signals shown
Note 2: Differential "P" cables will have differential signals on pins 1 - 34, except for DIFFSENS on pin 16.

28. SCSI Signals

ACK* Acknowledge. The initiator asserts this line low when it acknowledges that it has received or supplied data to the target (previously asserted REQ low for data response). Used in all asynchronous REQ/ACK data transfers.

ATN* Attention. Initiator driven.

BSY* Busy. OR-tied (on each device) line that indicates the bus is in use. Asserted low by either the initiator, the target, or both.

C/D* Control/Data. When low, indicates that control information is on the bus. When high, data is present on the bus. Target driven.

DB*<0-7> Data Bits 0-7. Bi-directional data bus. During Arbitration, Selection, and Reselection, these lines are used to transmit the device ID's, with each data bit corresponding to a different device number.

DBP* Data Bit Parity. Part of the data bus, but its use is optional in SCSI-1. Odd parity. Must be TRUE during arbitration.

DIFFSENS Differential Sense. Used on differential SCSI bus only. Enables the differential drivers.

I/O* Input/Output Direction. Direction of data transfer relative to initiator (input means: to the initiator). Also used to determine Selection and Reselection phases (asserted low during Reselection). Target driven.

MSG* Message. Indicates that the target has placed a message on the data bus.

REQ* Request. Target driven. Asserted low when target is ready to begin asynchronnous handshaking with the initiator.

RST* Reset. OR-tied line that indicates Reset condition.

SEL* Select. Used by the initiator to select a target device, and used by the target to reselect an initiator.

TRMPWR Terminator Power. Supplies power to terminating resistors at the ends of the bus.

29. IDE (ATA) Cable

Signal Name	Direction	Pin #
RESET*	>	1
GND		2
DD7	◇	3
DD8	◇	4
DD6	◇	5
DD9	◇	6
DD5	◇	7
DD10	◇	8
DD4	◇	9
DD11	◇	10
DD3	◇	11
DD12	◇	12
DD2	◇	13
DD13	◇	14
DD1	◇	15
DD14	◇	16
DD0	◇	17
DD15	◇	18
GND		19
KEY PIN		20
DMARQ	<	21
GND		22
DIOW*	>	23
GND		24
DIOR*	>	25
GND		26
IORDY	<	27
Reserved		28
DMACK*	>	29
GND		30
INTRQ	<	31
IOCS16*	<	32
DA1	>	33
PDIAG*	**	34
DA0	>	35
DA2	>	36
CS1FX*	>	37
CS3FX*	>	38
DASP*	<	39
GND		40

* = Active low
> = To drive from controller
< = To controller from drive
** = Drive to drive intercommunication

Cable: 40 pin flat or twisted, 3M 3365-40 or equivalent
Connector: 40 pin IDC , Molex 7723 40 A 587 or equivalent
No terminations required

30. IDE (ATA) Signals

CS1FX* Chip Select Drive 0. Used to select the host-accessable Command Block Register.

CS3FX* Chip Select Drive 1. Used to select the host-accessable Command Block Register.

DA0-2 Drive Address Bus. Address used by the host to access a register or the data port in the drive.

DASP* Drive Active/Drive 1 Present. Indicates drive activity or that drive 1 is present. This is a time multiplexed signal, which is first asserted by drive 1 (if present) and then by drive 0 (to drive an activity LED).

DD<0-15> Drive Data Bus. An 8 or 16 bit bi-directional data bus between the host and the drive. The lower 8 bits are used for 8 bit transfers (ECC bytes, for example).

DIOR* Drive I/O Read. Strobe signal for read functions. Negative edge enables data from a register or data port of the drive onto the host data bus. Positive edge latches data at the host.

DMACK* DMA Acknowledge. Used by the host to acknowledge that data has been accepted or data is available. Used in response to DMARQ asserted.

DMARQ DMA Request. Used for DMA transfers between host and drive (direction of transfer controlled by DIOR* and DIOW*). Used in an asynchronous mode with DMACK*. Drive asserts DMARQ when ready to transfer or receive data; drive waits until host asserts DMACK* before negating DMARQ and sending 16 bit word.

INTRQ Drive Interrupt Request. Asserted by drive when it has a pending interrupt (PIO transfer of data to or from the drive to the host).

IOCS16* Drive 16 bit I/O. Indicates to the host system that the 16 bit data port has been addressed and that the drive is prepared to send or receive a 16 bit data word.

IORDY I/O Channel Ready (optional). When negated, extends the host transfer cycle of any host register access when the drive is not ready to respond to a data transfer request. High impedance if asserted.

30. IDE Signals (cont.)

PDIAG* Passed Diagnostics. Output from drive 1 and monitored by drive 0. Provides an indication of the results of a diagnostics command or reset.

RESET* Resets the drive to the power on state.

Note concerning XT IDE drives: Although most of the IDE drives have been manufactured for the AT, there are a few versions for the XT. The XT drives are equivalent in all respects except for the use of only 8 data lines instead of 16. *Because the remaining 8 data lines are typically grounded, these XT drives should not be connected to the AT bus or to an AT bus extender card!*

31. POST Notes

The Power On System Test (POST) routines in the BIOS perform tests and initialize the circuitry on the motherboard and on peripheral adapter boards. The POST is reached by powering-on or using the CTRL-ALT-DEL re-boot keystrokes. From the reset state, program execution begins at the beginning of the highest paragraph of memory (F000:FFF0 for an 8088, FFFFF:00000 for an 80286+) with a long jump to E000:E05B, where the POST sequence starts. The degree and manner of test/initialization will vary among the different brands of BIOS.

The usual sequence is:

- Do some CPU register checks
- Setup the 8253/8254 timer for RAM refresh timing
- Setup the DMA for RAM refresh on channel 0
- Verify that refresh is operating
- Test the low RAM (16-64K)
- Load Interrupt Vectors and assign a stack in the low RAM area.
- Initialize video and keyboard devices
- Size and test the remaining RAM
- Initialize the COM, LPT, and Game Ports
- Initialize the floppy disk system
- Initialize the hard disk system (for ATs)
- Scan the User ROM area (see next section)
- Call the Bootstrap Interrupt

32. User ROM Scan

The BIOS provides a means whereby builders of adapter cards may hook into the power-on initialization sequence.

During POST, the BIOS loads a set of default vectors into the appropriate BIOS interrupt addresses. Then the BIOS scans memory addresses C8000 to F4000 in 2K blocks looking for valid modules on the I/O bus.

A valid module will have 55H as byte 0, AAH as byte 1, and a length indicator in byte 2. The length byte is the number of 512 byte blocks over which a checksum (modulo hex 100) must be zero. (The length byte must not exceed FBh, regardless of the length of your code, so you must force a sum of 00 starting with byte 0 up to whatever length byte 2 represents. Your actual code may be longer, but an error will occur if the length byte is larger than FBh.)

Your initialization code must start in Byte 3, since the BIOS will do a Far Call there if the module is found to be valid (passes the three tests above). If you will want control back later when the computer boots, this is also your chance to change the boot vector to point to the entry point for your code. At the end, do a Far Return so the BIOS can finish the power-on routines. If you have changed the boot vector to point to your entry point, you will regain control when the computer boots.

If your module is correct, it will start with 55 AA, and will have a checksum of 00 over the distance indicated by the length code in byte 2. (The length code will be divisible by four.)

33. Memory Map

Hex Address Range		Usage
00000-9FFFF	(640K)	System DRAM
00000-001DF	(480)	Interrupt Vectors
001E0-002FF	(288)	User Vectors
00300-003FF	(256)	Bios Stack/User Vectors
00400-004FF	(256)	Bios Data
00500-005FF	(256)	DOS and Basic Use
00600-9FFFF	(638K)	User Ram
A0000-BFFFF	(128K)	Video Buffer RAM Area
A0000-BFFFF	(128K)	EGA/VGA Video Buffer
B0000-B7FFF	(32K)	MDA Video Buffer
B8000-BFFFF	(32K)	CGA Video Buffer
C0000-DFFFF	(128K)	Rom Expansion Area
C0000-C3FFF	(16K)	EGA Bios
C6000-C63FF	(1K)	PGA Comm Area
C8000-CBFFF	(16K)	XT Hard Disk Bios
D0000-D7FFF	(32K)	Cluster Adapter Bios
E0000-EFFFF	(64K)	Rom Expansion (XT) Bios Expansion (AT)
F0000-FFFFF	(64K)	BIOS
100000-FDFFFF	(14.9MB)	AT Extended RAM
FE0000-FFFFFF	(128K)	AT Rom Bios Area

34. I/O Map

Hex Range	Usage
000-00F	8237 DMA Controller #1
020-021	8259 Master Interrupt Controller
040-043	8253 Programmable Interrupt Timer
060-06F	8042 Keyboard Controller
070-07F	CMOS RAM, NMI Mask Reg, RT Clock
080-09F	DMA Page Registers
0A0-0BF	8259 Slave Interrupt Controller
0C0-0DF	8237 DMA Controller #2
0F0-0F1	Math Coprocessor
0F8-0FF	Math Coprocessor
170-177	Fixed Disk Controller #2
1F0-1F8	Fixed Disk Controller #1
200-207	Game Portl
238-23B	Bus Mouse
23C-23F	Alt. Bus Mouse
278-27F	Parallel Printer
2B0-2BF	EGA
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	Serial Port
2F8-2FF	Serial Port
300-30F	Prototype Card
310-31F	Prototype Card
320-32F	Hard Disk (XT)
370-377	Floppy Controller #2
378-37F	Parallel Printer
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	Parallel Printer
3C0-3CF	VGA EGA
3D0-3DF	CGA
3E8-3EF	Serial Port
3F0-3F7	Floppy Controller #1
3F8-3FF	Serial Port

Due to the wide variety of third-party adapters available for the PC-Bus, the installation of adapters using ports not listed above may result in conflicting assignments. Users are cautioned that problems usually occur if ports collide.

35. BIOS Data Area

The Bios Data area is located at 0040:0000 - 0040:00FF. The table below shows the typical usage. Locations shown as "not used" or "reserved" may in fact be used in some instances.

Loc.	Size	Description
00	word	COM1 port address
02	word	COM2 port address
04	word	COM3 port address
06	word	COM4 port address
08	word	LPT1 port address
0A	word	LPT2 port address
0C	word	LPT3 port address
0E	word	Extended Bios Data Pointer
10	word	equipment variable
12	byte	manufacturing test
13	word	memory size in 1K blocks
15	word	error codes
17	byte	keyboard shift flag 1
18	byte	keyboard shift flag2
19	byte	ALT-keypad buffer
1A	word	keyboard buffer head
1C	word	keyboard buffer tail
1E	16 words	keyboard buffer
3E	byte	floppy recalibrate flag
3F	byte	floppy motor status
40	byte	floppy motor off counter
41	byte	floppy status byte
42	7 bytes	floppy controller status bytes
49	byte	display mode
4A	word	display number of columns
4C	word	video buffer length (bytes)
4E	word	video current page
50	8 words	cursor position (8 pages)
60	word	cursor type
62	byte	active display page
63	word	video controller port address
65	byte	current 3x8 register value
66	byte	current 3x9 register value
67	dword	virtual save for segment:offset
6B	byte	virtual mode flag
6C	dword	timer counter
70	byte	timer overflow flag
71	byte	break key flag
72	word	reset flag (1234H = warm boot)
74	byte	hard disk status

35. BIOS Data Area (cont.)

75	byte	number of hard drives
76	byte	XT hard disk control byte
77	byte	XT hard disk controller port
78	byte	LPT1 timeout value
79	byte	LPT2 timeout value
7A	byte	LPT3 timeout value
7B	byte	LPT4 timeout value
7C	byte	COM1 timeout value
7D	byte	COM2 timeout value
7E	byte	COM3 timeout value
7F	byte	COM4 timeout value
80	word	keyboard buffer start pointer
82	word	keyboard buffer end pointer
84	byte	number of video rows (-1)
85	word	char height in bytes/char
87	byte	video options
88	byte	video switches
89	byte	video save area 1
8A	byte	video save area 2
8B	byte	floppy data and step rates
8C	byte	hard disk controller status
8D	byte	hard disk error status
8E	byte	hard disk interrupt control
8F	byte	floppy controller info
90	byte	floppy drive 0 media state
91	byte	floppy drive 1 media state
92	byte	floppy drive 0 media state
93	byte	floppy drive 1 media state
94	byte	floppy drive 0 current cylinder
95	byte	floppy drive 1 current cylinder
96	byte	keyboard flag 3
97	byte	keyboard LED flags
98	dword	vector to user wait flag
9C	dword	user wait count
A0	byte	wait active flag
A1	7 bytes	LAN
A8	dword	EGA parameter table pointer
AC	dword	EGA save area 1 pointer
B0	dword	EGA alpha font pointer
B4	dword	EGA graphics font pointer
B8	dword	PS/2 save area 2 pointer
BC	72 bytes	reserved

0050:0000 is the print_screen status byte

36. Interrupt Map

No.	Addr	Type	Description
0	00	CPU	Divide by Zero
1	04	CPU	Single Step
		386+	Debug Exception
2	08	CPU	NMI
3	0C	CPU	Breakpoint
4	10	CPU	Overflow
5	14	Bios	Print Screen
		186+	Bounds Fault Exception
6	18	186+	Invalid Opcode
7	1C	186+	NPX unavailable
8	20	Bios	IRQ0 - Time of Day
		286+	LIDT or Double Fault
9	24	Bios	IRQ1 - Keyboard
		286+	NPX segment
A	28	Bios	IRQ2 - Reserved
		286+	Invalid TSS
B	2C	Bios	IRQ3 - COM 2
		286+	Segment not present
C	30	Bios	IRQ4 - COM 1
		286+	Stack Fault Exception
D	34	Bios	IRQ5 - XT-Hard Disk, AT-LPT
		286+	Protection Fault
E	38	Bios	IRQ6 - Floppy Disk
		386+	Page Fault
F	3C	Bios	IRQ7 - LPT
10	40	Bios	Video Driver
		286+	NPX Error
11	44	Bios	Equipment Check
		486+	Alignment Check
12	48	Bios	Memory Size
		Pentium	Machine check
13	4C	Bios	Disk Driver
14	50	Bios	Serial Driver
15	54	Bios	Cassette Driver
16	58	Bios	Keyboard Driver
17	5C	Bios	Printer Driver
18	60	Bios	BASIC (SysVue)
19	64	Bios	Bootstrap
1A	68	Bios	Time of Day
1B	6C	Bios	Keyboard Break
1C	70	Bios	Timer Tick
1D	74	Bios	Video Initialization
1E	78	Bios	Diskette Parm Table

36. Interrupt Map (cont.)

1F	7C	Bios	CGA Graphics Font
20	80	DOS	Program Terminate
21	84	DOS	Function Call
22	88	DOS	Terminate Address
23	8C	DOS	Ctrl-Brk Exit Address
24	90	DOS	Fatal Error Vector
25	94	DOS	Absolute Disk Read
26	98	DOS	Absolute Disk Write
27	9C	DOS	Terminate
28	A0	DOS	Idle Signal
29	A4	DOS	TTY Output
2A	A8	DOS	MS-Net services
2F	BC	DOS	Print Spool
30	C0	DOS	Long Jump interface
33	CC	DOS	Mouse Functions
3F	FC	DOS	Overlay Interrupt
40	100	Bios	Hard Disk Chain
41	104	Bios	Disk #1 Parm Table
42	108	Bios	EGA Chain
43	10C	Bios	EGA Parm Table Ptr
44	110	Bios	EGA Graphics Font
46	118	Bios	Disk #2 Parm Table
4A	128	Bios	AT Alarm Exit Address
50	140	Bios	AT Alarm Interrupt
51	144	Bios	Mouse Functions
5A	168	NET	Functions
5B	16C	NET	Boot Chain
5C	170	NET	NetBios entry
67	19C	DOS	EMS Functions
6D	1B4	VGA	Suspected VGA Service
70	1C0	ATBios	IRQ8 - Real-Time Clock
71	1C4	ATBios	IRQ9 - Re-directed to IRQ2
72	1C8	ATBios	IRQ10 - Unassigned
73	1CC	ATBios	IRQ11 - Unassigned
74	1D0	ATBios	IRQ12 - Unassigned
75	1D4	ATBios	IRQ13 - 80287 NPX
76	1D8	ATBios	IRQ14 - AT Hard Disk
77	1DC	ATBios	IRQ15 - Unassigned
80-F0	200-3C0	BASIC	
F1-FF	3C4-3FC	—	Not Used

37. Hardware Interrupts

Name	Int#	Description
NMI	02	Parity* (highest priority)
0	08	Timer* (8253 TMR0)
1	09	Keyboard*
IRQ2	0A	Cascade; Int. 8-15
IRQ3	0B	Serial Port or SDLC
IRQ4	0C	Serial Port or SDLC
IRQ5	0D	Parallel Port
IRQ6	0E	Floppy Disk
IRQ7	0F	Parallel Port (lowest priority)
IRQ8	70	CMOS Real-Time Clock
IRQ9	71	Re-directed to IRQ2
IRQ10	72	Unassigned
IRQ11	73	Unassigned
IRQ12	74	Mouse or other
IRQ13	75	Math Coprocessor
IRQ14	76	Hard Disk
IRQ15	77	Unassigned

*These interrupts exist on the system board and are not available on the bus connector.

38. DMA Channels

Channel	Usage
0	Memory Refresh
1	SDLC
2	Floppy Disk
3	Unassigned
4	DMA Cascade Line; Not Available
5	Unassigned
6	Unassigned
7	Unassigned

Channels 0-3 (DMA #1) are 8 bit channels (XT & AT).

Channels 4-7 (DMA #2) are 16 bit channels (AT only).

39. BIOS Entry Points

IBM has always warned programmers not to use the actual entry points for the various BIOS routines, as they may change from version to version. The proper entry to the BIOS is through the software interrupt system. In practice, however, usually in the interest of maximizing speed, there have been those who violate the rule. The following entry points have remained constant on all or nearly all of the PC compatible BIOS versions. Be aware of the risk to future compatibility if your software uses them.

Address	Name
F000:E05B	Reset
F000:E2C3	NMI Entry Point
F000:E6F2	Bootstrap Load
F000:E729	UART Parms for Overlaying Drivers
F000:E739	Comm Function Call
F000:E82E	Keyboard Function Call
F000:E987	Keyboard Hardware Interrupt
F000:EC59	Floppy Disk Function Call
F000:EF57	Floppy Disk ISR
F000:EFC7	Floppy Disk Parameter Table
F000:EFD2	LPT Function Call
F000:F065	Video Function Call
F000:F0A4	Video 6845 Parameters
F000:F841	Memory Size Function Call
F000:F84D	Equipment Check Function Call
F000:F859	Cassette Function Call
F000:FA6E	Video Char. Font-Graphics Mode
F000:FE6E	Timer Function Call
F000:FEA5	Timer Hardware Interrupt
F000:FEF3	Interrupt Vector Table
F000:FF53	Dummy Interrupt Return
F000:FF54	Print Screen Function Call
F000:FFF0	Hardware Reset Point
F000:FFF5	Date Stamp of BIOS
F000:FFFE	Hardware ID Byte (Model Number)

FF = PC
FE = XT and Portable PC
FD = PCjr
FC = AT
FB = XT After 1-10-86
FA = PS/2 Model 30
F9 = PC Convertible
F8 = PS/2 Model 80

40. CMOS Memory and Real-Time Clock

Real time clock is BCD values in locations 00-0D.

00 Seconds
01 Seconds Alarm
02 Minutes
03 Minutes Alarm
04 Hours
05 Hours Alarm
06 Day of Week
07 Day of Month
08 Month
09 Year

0A Bit 7 - Update in Progress

0E is the Diagnostic Status Byte:
Bit 7 - Chip lost power
Bit 6 - Bad checksum
Bit 5 - Bad configuration byte
Bit 4 - Bad memory size
Bit 3 - Bad hard disk byte
Bit 2 - Bad time of day

0F is the restart status byte. It is loaded before doing a re-start of the 80286, such as when returning from protected mode.

10 designates the floppy disk drive type:
Bits 7-4 Drive A:
Bits 3-0 Drive B:
0 No drive
1 360K drive
2 1.2 MB drive
3 720K drive
4 1.44 MB drive

12 is the hard disk drive type:
Bits 7-4 1st Hard Drive
Bits 3-0 2nd Hard Drive
0 No drive
1-E Type 1-15
F Use contents of byte 19 or 1A.

40. CMOS Memory (cont.)

14 is the equipment byte:
Bits 7-6: 00 = 1 Floppy
01 2 Floppies
10 3 Floppies (AT BiosKit)
11 4 Floppies (AT BiosKit)
Bits 5-4: 00 = EGA/VGA
01 CGA 40 x 25
10 CGA 80 x 25
11 MDA

Bit 1: 80287 installed
Bit 0: Floppy drive(s) present

15-16 are the memory size below 1MB (preset by setup program)

17-18 are the memory size above 1MB (preset by setup program)

19 1st Hard Disk type when 12(Bits 7-4) = type F

1A 2nd Hard Disk type when 12(Bits 3-0) = type F

2E-2F are the checksum for bytes 10-2D.

30-31 indicate the memory size above 1MB as determined by power-up routines.

32 is the BCD century byte

33 indicates the power-on information flags:
Bit 7 Top 128K of RAM is installed (shadow RAM is available).
Bit 6 First bootup after running setup routine.

To read or write to the AT's CMOS memory:
Output cell address to I/O port 70.
Read/Write data from/to I/O port 71.

41. Video

CGA Board:

3D4 **6845 Address Register**
3D5 **6845 Data Register**
3D8 **Control Register-Write**
Bit 5 - Background Intensity/Blink Selector
Bit 4 - Disable/Enable 640 x 200 B/W Mode
Bit 3 - Disable/Enable Video
Bit 2 - Color/B/W Mode
Bit 1 - Text/Graphics Mode
Bit 0 - 40 x 25/80 x 25 Mode
3D9 **Color Select Register-Write**
Bit 7 - Not used
Bit 6 - Not used
Bit 5 - Active Color Set (320x200)
Bit 4 - Intensified
Alternate Color Set (Graphics)
Background Colors (Alphanumeric)
Bit 3 - Selects Intensified:
Border Color (40x25)
Background Color (320x200)
Foreground Color (640x200)
Bit 2 - Selects Red:
Border Color (40x25)
Background Color (320x200)
Foreground Color (640x200)
Bit 1 - Selects Green:
Border Color (40x25)
Background Color (320x200)
Foreground Color (640x200)
Bit 0 - Selects Blue:
Border Color (40x25)
Background Color (320x200)
Foreground Color (640x200)
3DA **Status Register-Read**
Bit 3 - Vertical Sync
Bit 2 - Light Pen Switch
Bit 1 - Light Pen Trigger Armed
Bit 0 - Display Enable

Buffer at B8000

41. Video (cont.)

EGA Board:

3C0	ATC Index register
3C2	Input Status register 0
3C4	TS Index Register
3C5	TS Data Register
3CA	Graphics position register 2
3CC	Graphics position register 1
3CE	GDC index register
3CF	GDC data register
3B4-3D4	CRTC index register
3B5-3D5	CRTC data register
3BA-3DA	Input status register 1

Buffer at A0000

VGA Board:

3C0	RW	Address register
3C0	W	Attribute register
3C1	R	Attribute register
3C2	R	Input Status register 0
3C2	W	Misc. output
3C3	RW	Video subsystem enable
3C4	RW	Address register
3C5	RW	Sequence register
3C6	RW	PEL mask register
3C7	RW	PEL address read mode
3C7	R	DAC state register
3C8	RW	PEL address write mode
3C9	RW	PEL data register
3CA	R	Feature control register
3CC	R	Misc output
3CE	RW	Address register
3CF	RW	Graphics register
3B4-3D4	W	CRTC index
3B5-3D5	RW	CRTC data
3BA-3DA	R	Input Status register 1
3BA-3DA	W	Feature Control register

Buffer at A0000

41. Video (cont.)

MDA Board:

3B4	6845 Address Register
3B5	6845 Data Register
3B8	Control Register-Write
	Bit 5 - Disable/Enable Blink
	Bit 3 - Disable/Enable Video
	Bit 0 - High Res. Mode
3BA	Status Register-Read
	Bit 7 - Vertical Sync
	Bit 3 - Video
	Bit 0 - Horizontal Sync

Buffer at B0000

Programming the 6845 Video Controller for Different Modes:
To set up the 6845, the Address Register 3X4 is loaded with the Register #, and the values in the following table are written to 3X5. Each column represents a different mode:

A: 40 x 25 Color-Text
B: 80 x 25 Color-Text
C: 320 x 400 / 640 x 200 Mode for Color Bd.
D: 80 x 25 Monochrome-Text
E: 80 x 25 Mono.-Hercules Graphics

Reg#	A	B	C	D	E
0	38	71	38	61	36
1	28	50	28	50	2D
2	2D	5A	2D	52	2F
3	0A	0A	0A	0F	07
4	1F	1F	7F	19	5B
5	06	06	06	06	00
6	19	19	64	19	57
7	1C	1C	70	19	57
8	02	02	02	02	02
9	07	07	01	0D	03
A	06	06	06	0B	00
B	07	07	07	0C	00
C	00	00	00	00	00
D	00	00	00	00	00

42. 8237 DMA Controllers

Controller 1: 8-bit (ports 000-00F)

Page Register	I/O Address
Channel 0	(AT) 087
Channel 1	083
Channel 2	081
Channel 3	082

Controller 2: 16-bit (AT Only - ports 0C0-0DF)

Page Register	I/O Address
Channel 5	08B
Channel 6	089
Channel 7	08A

Refresh (AT) 08F

DMA# 1	2	Description
000	0C0	Channel 0/4 Base & Current Address
001	0C2	Channel 0/4 Base & Current Word Count
002	0C4	Channel 1/5 Base & Current Address
003	0C6	Channel 1/5 Base & Current Word Count
004	0C8	Channel 2/6 Base & Current Address
005	0CA	Channel 2/6 Base & Current Word Count
006	0CC	Channel 3/7 Base & Current Address
007	0CE	Channel 3/7 Base & Current Word Count
008	0D0	Read Status/Write Command Register
009	0D2	Write Request Register
00A	0D4	Write Single Mask Register Bit
00B	0D6	Write Mode Register
00C	0D8	Clear Byte Pointer Flip/Flop
00D	0DA	Read Temp Regsiter/Write Master Clear
00E	0DC	Clear Mask Register
00F	0DE	Write All Mask Register Bits

43. 8042 Keyboard Controller

Instead of the 8255 PIO used in the PC/XT, the AT uses an 8042 Keyboard Controller at ports 60 and 64, and an emulated read/write port at 61 to perform similar functions.

Hex		Name	Description
60		**Data**	**8042 KB Controller Data Port**
61		**Status**	**Emulated 8255 R/W Port B**
Bit 7	r	PCK	System memory parity check
Bit 6	r	CHK	I/O channel check
Bit 5	r	T2O	Timer 2 output
Bit 4	r	RFD	Refresh Detect
Bit 3	r/w	EIC	enable I/O channel check
Bit 2	r/w	ERP	enable memory parity check
Bit 1	r/w	SPK	speaker data
Bit 0	r/w	T2G	Timer 2 gate (speaker)

64 Control/Status 8042 KB Controller

Control Commands

20	Read Controller
60	Write Controller
AA	Self Test
AB	Interface Test
AC	Diagnostic Dump
AD	Disable Keyboard
AE	Enable Keyboard
C0	Read Discrete Input Port
D0	Read Discrete Output Port
D1	Write Discrete Output Port
E0	Read T0 and T1 inputs
F0-FF	Pulse Discrete Output Port

Status Inputs

Bit 7	1 = Parity Error
Bit 6	1 = RX Timeout
Bit 5	1 = Tx Timeout
Bit 4	1 = KB Inhibited
Bit 3	1 = Command, 0 = Data
Bit 2	1 = Reset OK, 0 = power on
Bit 1	1 = input buffer full
Bit 0	1 = output buffer full

43. 8042 Keyboard Controller (cont.)

The AT KB controller also has a discrete input port and a discrete output port. These are accessed with the read/write port commands and are used as follows:

Discrete Input Port

Bit 7	KB Inhibit Switch, 0 = locked
Bit 6	Video Default, 0 = CGA, 1 = MDA
Bit 5	MFG Jumper, 0 = jumper, 1 = no jumper
Bit 4	System RAM, 0 = 512K, 1 = 256K

Discrete Output Port

Bit 7	KB Serial Data Out
Bit 6	KB Serial Clock Out
Bit 5	Input Buffer Empty, 0 = full, 1 = empty
Bit 4	Output Buffer Empty, 0 = empty, 1 = full
Bit 1	Gate A20
Bit 0	System Reset

44. 8259 Interrupt Controllers

Note: The 8259 Programmable Interrupt Controller accesses an internal register set through two I/O ports. The 8259 is initialized by loading up to a 4-byte configuration sequence. It then responds in an Operation Mode. Configuration bytes may vary somewhat due to hardware implementations. The port usage shown below is in the Operation Mode.

For 8259 #1 (AT and XT)
Interrupt Controller #1 Ports are 20-21
Interrupts are positive-edge sense.
Port 20 is used to acknowledge and re-enable the 8259
To send non-specific end-of-interrupt code:

```
mov  al,20h
out  20h,al
```

Port 21 is used to set/clear the masking register
A Mask Bit = 0 => enable, 1 => disable a specific IRQ
To read Interrupt Mask Register

```
in   al,21h Bit 7-0 = IRQ 7-0
```

To write Interrupt Mask Register

```
mov  al,mask
out  21h,al
```

For 8259 #2 (AT Only)
Interrupt Controller #2 Ports are A0-A1
Interrupts are positive-edge sense.
Port A0 is used to acknowledge and re-enable the 8259
To send non-specific end-of-interrupt code:

```
mov  al,20h
out  0A0h,al
```

Port A1 is used to set/clear the masking register
A Mask Bit = 0 => enable, 1 => disable a specific IRQ
To read Interrupt Mask Register

```
in   al,0A1h    Bit 7-0 = IRQ 15-8
```

To write Interrupt Mask Register

```
mov  al,mask
out  0A1h,al
```

45. 8253/8254 Counter/Timer

Port	Section	Description
40	Counter 0	**Real Time Clock Tick** Count = 1000h Output to IRQ0 every 54.9255 ms. (approx. 18.2 ticks per second, 1,573,040 (1800B0h) per day) Mode = LSB-MSB, 3, binary
41	Counter 1	**DRAM Refresh** Count = 0012h Output to DRQ0 (XT) Refresh Logic (AT) (Refresh approx every 15 usec.) Mode = LSB, 2, binary
42	Counter 2	**Speaker Oscillator** Gated by Bit 0 of 8255 Port B Mode = LSB-MSB, 3, binary
43	**Control Register** Bit 7, 6 Select Counter 0, 1, 2 Bit 5, 4 Latch, LSB, MSB, LSB-MSB Bit 3, 2, 1 Mode 0 - Interrupt on count 1 - One-shot 2 - Rate generator 3 - Square Wave generator 4 - Triggered strobe (software) 5 - Triggered strobe (hardware) Bit 0 Binary/BCD counting	

Note: The internal count registers of the 8253/8254 operate in a down-counter mode. If reading register counts for high-resolution timing routines, each count from counter 0 is = 1/1.19318MHz, or .8380966 usecs. A reload (after the count reaches zero) occurs every 54.9255 milliseconds.

46. 8250 Serial Chip Notes

PC Serial Ports may be implemented with a variety of chips, all variations of the 8250 architecture. There are some differences between members of the 8250 family, however, which may cause operational anomalies. The common chip types are labeled:

INS8250
INS8250-B
INS8250A
INS82C50A
NS16450
NS16C450
NS16550A

The INS8250 and INS8250-B had slow access cycle delays, requiring extra NOPS between CPU read/write cycles.

The INS8250 had an "interrupt pending" glitch which was corrected on later versions.

The INS8250A corrected some bugs, which were desired by BIOS coding, possibly making them incompatible with some software packages.. The scratch register (#7) was included on the INS8250A and NS16450/16C450/16550A versions.

The NS16550A includes TX and RX FIFO's, DMA interface, and higher baud rates.

When selecting or replacing 8250 family chips, the preferred type is one of the 16550 series.

47. 8250 Register Description

Register	Reg#	7	6	5	4	3	2	1	0
DATA	0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DLL	0	Baud Rate Gen. LSB Divide Count (DLAB = 1)							
DLH	1	Baud Rate Gen. MSB Divide Count (DLAB = 1)							
IER	1	0	0	0	-	Modem Int. Enab.	Rx line Int. Enab.	Tx data Int. Enab.	Rx Data Int. Enabl
IIR	2	0	0	0	0	0	Active Int. Bit 0	Active Int. Bit 1	Int. Pending
LCR	3	DLAB Divisor Latch Bit	Set Break Bit 2	Parity Mode Bit 1	Parity Mode Bit 0	Parity Enable	Stop Bit Length Bit 1	Char Length Bit 0	Char Length Bit 1
MCR	4	0	0	0	Loopback	-OUT2	0	-RTS	DTR
LSR	5	0	TEMT	THRE	Break	Framing	Parity	Overrun	Rx Rdy
MSR	6	DCD	RE	DSR	CTS	DDCD	TERI	DDSR	DCTS
SCR	7	Scratch-Pad Register							

48. Logical & Physical Devices

There is often confusion about the logical names COM1-4, LPT1-3 and their physical I/O addresses. For example, LPT1: is not always found at the same address. The reason is that the port addresses are scanned by the BIOS in a particular order, and the first device found is labeled #1. The port addresses found this way are stored in a device list. Therefore a particular physical address does not guarantee that a device will be assigned a particular device number. The order in which the physical devices are scanned is:

COM Ports: 3F8, 2F8, 3E8, 2E8
LPT Ports: 3BC, 378, 278
To inspect the port lists, use DEBUG:
d 40.0 7 = COM list
d 40:8 F = LPT list

49. Bi-Directional Parallel Port

Because of the wiring of the port chip, data can normally only be input through the port a nibble at a time by using four of the five status register input lines. MS-DOS Interlink uses this method. IBM has better methods on the PS/2, and Intel has a chip (see Section 21). IEEE is working on a standard (1284). For more information, see *The Personal Computer from the Inside Out*, available from Annabooks.

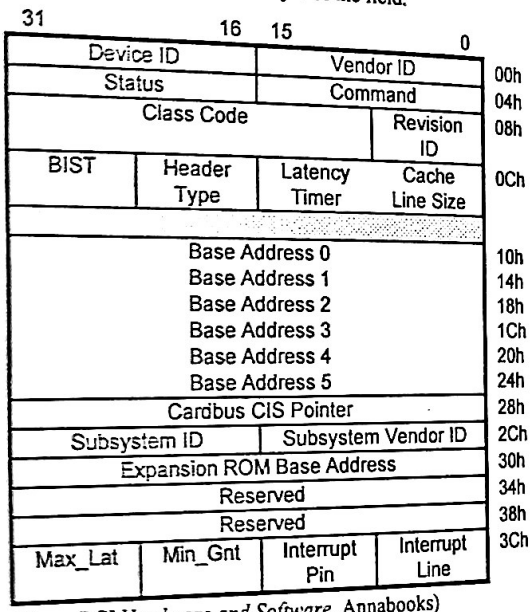
50. Enhanced (Fast) Parallel Port

The Fast parallel port design allows transfers up to 2 Mbytes/sec. Intel supports it (called the Enhanced Parallel Port-EPP) on the 386SL and 486 SL. For more information, GO IRUG on CompuServe. The following five pins change function:

Pin	Standard Function	EPP Function
1	-Strobe	-Write
10	-Acknowledge	-Interrupt Request
11	+Busy	-Wait
14	-Paper Feed	-Data Strobe
17	-Select	-Address Strobe

51. PCI Configuration Space Header Type 00h

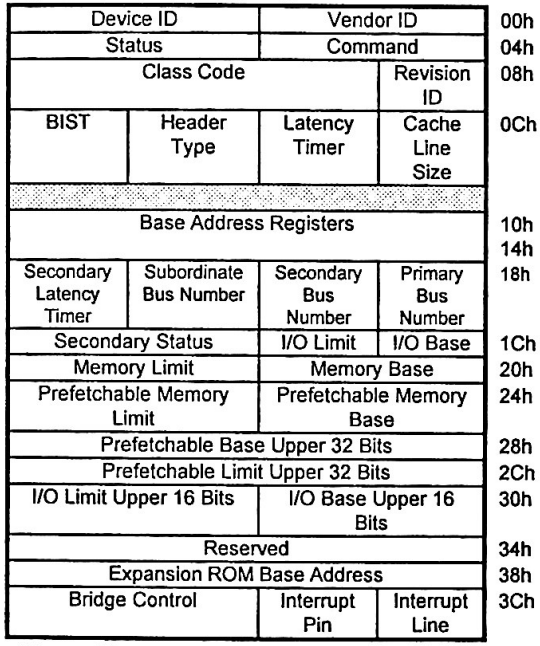
This is a pictorial view of the 64 byte register layout of Type 00h PCI Configuration Space Header. All PCI compliant devices that implement a Type 00h header must support this layout. Fields that utilize more than one byte in this structure follow little–endian ordering. For example, the least significant byte of the two-byte Vendor ID field is contained in the bottommost byte of the field.



(From *PCI Hardware and Software*, Annabooks)

52. PCI Configuration Space Header Type 01h

This is a pictorial view of the 64 byte register layout of Type 01H PCI Configuration Space Header. All PCI compliant devices that implement a Type 01H header must support this layout. Fields that utilize more than one byte in this structure follow little–endian ordering. For example, the least significant byte of the two-byte Vendor ID field is contained in the bottommost byte of the field.



(From *PCI Hardware and Software*, Annabooks)

53. PC Card (PCMCIA) Socket Services

Call PC Card Socket Services with INT 1Ah (functions 80h and higher:

Adapter Functions	
GetAdapterCount	80h
Reserved	81h
Reserved	82h
GetSocketServiceInfo	83h
InquireAdapter	84h
GetAdapter	85h
SetAdapter	86h
Window Functions	
InquireWindow	87h
GetWindow	88h
SetWindow	89h
GetPage	8Ah
SetPage	8Bh
Socket Functions	
InquireSocket	8Ch
GetSocket	8Dh
SetSocket	8Eh
Card Functions	
GetStatus	8Fh
ResetSocket	90h
Reserved	91h
to	9Ch

Vendor Specific Functions	
GetVendorInfo	9Dh
VendorSpecific	AEh
Protect-Mode and Low-Level Access	
Get/SetPriorHandler	9Fh
Get/SetSSAddr	A0h
GetAccessOffsets	A1h
AcknowledgeInterrupt	9Eh
Error Detection and Correction Functions	
GetEDC	NA
InquireEDC	NA
PauseEDC	NA
ReadEDC	NA
ResumeEDC	NA
SetEDC	NA
StartEDC	NA
StopEDC	NA

From *Designing With Flash Memory*, Annabooks.

54. PC Card (PCMCIA) Card Services

Card Services are accessed through INT 1Ah, function AFh.

CloseMemory	00h
DeregisterClient	02h
GetConfigurationIn	04h
GetFirstRegion	06h
GetNextPartition	08h
GetNextTuple	0Ah
GetStatus	0Ch
GetFirstClient	0Eh
RegisterClient	10h
MapLogSocket	12h
MapMemPage	14h
MapPhyWindow	16h
OpenMemory	18h
RegisterMTD	1Ah
ReleaseIRQ	1Ch
ReleaseConfigurati	1Eh
RequestIRQ	20h
RequestSocketMas	22h
WriteMemory	24h
CheckEraseQueue	26h
RegisterTimer	28h
GetNextClient	2Ah
RequestExclusive	2Ch
GetEventMask	2Eh
RequestConfigurati	30h
AddSocketServices	32h
AdjustResourceInfo	35h
AccessConfigurationRegist	36h

CopyMemory	01h
GetClientInfo	03h
GetFirstPartition	05h
GetFirstTuple	07h
GetNextRegion	09h
GetCardServicesInf	0Bh
GetTupleData	0Dh
RegisterEraseQueu	0Fh
ResetCard	11h
MapLogWindow	13h
MapPhySocket	15h
ModifyWindow	17h
ReadMemory	19h
ReleaseIO	1Bh
ReleaseWindow	1Dh
RequestIO	1Fh
RequestWindow	21h
ReturnSSEntry	23h
DeregisterEraseQu	25h
ModifyConfigurati	27h
SetRegion	29h
ValidateCIS	2Bh
ReleaseExclusive	2Dh
ReleaseSocketMas	2Fh
SetEventMask	31h
VendorSpecific	34h

55. AT-84 Key Keyboard Scan Codes

Key #	Scan Code	Base Case	Upper Case	CTRL	ALT
1	0E	`	~	-	-
2	16	1	!	-	ext
3	1E	2	@	NUL	ext
4	26	3	#	-	ext
5	25	4	$	-	ext
6	2E	5	%	-	ext
7	36	6	^	RS	ext
8	3D	7	&	-	ext
9	3E	8	*	-	ext
10	46	9	(	-	ext
11	45	0	)	-	ext
12	4E	-	_	US	ext
13	55	=	+	-	ext
14	5D	\	|	FS	-
15	56	Bspace	Bspace	DEL	-
16	0D	Tab	Ext	-	-
17	15	q	Q	DC1	ext
18	1D	w	W	ETB	ext
19	24	e	E	ENQ	ext
20	2D	r	R	DC2	ext
21	2C	t	T	DC4	ext
22	35	y	Y	EM	ext
23	3C	u	U	NAK	ext
24	43	i	I	HT	ext
25	44	o	O	SI	ext
26	4D	p	P	DLE	ext
27	54	[	{	ESC	-
28	5B	]	}	GS	-
30	14	Ctrl	-	-	-
31	1C	a	A	SOH	ext
32	1B	s	S	DC3	ext
33	23	d	D	EOT	ext
34	2B	f	F	ACK	ext
35	34	g	G	BEL	ext
36	33	h	H	BS	ext
37	3B	j	J	LF	ext
38	42	k	K	VT	ext
39	4B	l	L	FF	ext
40	4C	;	:	-	-
41	52	'	"	-	-
43	5A	Enter	Enter	LF	-
44	12	Lt Shift	-	-	-
46	1A	z	Z	SUB	ext
47	22	x	X	CAN	ext
48	21	c	C	ETX	ext

55. AT-84 Key Keyboard (cont.)

49	2A	v	V	SYN	ext
50	32	b	B	STX	ext
51	31	n	N	SO	ext
52	3A	m	M	CR	ext
53	41	,	<	-	-
54	49	.	>	-	-
55	4A	/	?	-	-
57	59	Rt Shift	-	-	-
58	11	Alt	-	-	-
61	29	Space	Space	Space	Space
64	58	Caps Lk	-	-	-
65	06	F2	ext	ext	ext
66	0C	F4	ext	ext	ext
67	0B	F6	ext	ext	ext
68	0A	F8	ext	ext	ext
69	09	F10	ext	ext	ext
70	05	F1	ext	ext	ext
71	04	F3	ext	ext	ext
72	03	F5	ext	ext	ext
73	B3	F7	ext	ext	ext
74	01	F9	ext	ext	ext
75	70	Insert	-	-	-
90	76	Esc	Esc	Esc	-
91	BC	Home	N/A	ext	-
92	6B	Lft	N/A	ext	-
93	69	End	N/A	ext	-
95	77	Num Lk	-	pause	-
96	75	Up	N/A	-	-
97	73	Pad 5	N/A	-	-
98	72	Dn	N/A	ext	-
99	70	Ins	N/A	-	-
100	7E	Scroll Lk	-	break	
101	7D	PgUp	N/A	ext	-
102	74	Rt	N/A	ext	-
103	7A	PgDn	N/A	ext	-
104	71	Del	-	*	*
105	78	sys req	-	-	-
106	7C	Pad *	prt scr	-	-
107	7B	Pad -	N/A	-	-
108	79	Pad +	N/A	-	-

NOTES: (See also Notes at end of Section 45)

ext = extended (returns 00 followed by scan code)

* Ctrl-Alt-Del = Warm Boot

Make (down-key) shown: Break followed by F0H

56. AT 101-Key Keyboard Scan Codes

Key #	Scan Code	Base Case	Upper Case	CTRL	ALT
1	0E	`	~	-	-
2	16	1	!	-	ext
3	1E	2	@	NUL	ext
4	26	3	#	-	ext
5	25	4	$	-	ext
6	2E	5	%	-	ext
7	36	6	^	RS	ext
8	3D	7	&	-	ext
9	3E	8	*	-	ext
10	46	9	(	-	ext
11	45	0	)	-	ext
12	4E	-	_	US	ext
13	55	=	+	-	ext
15	56	Bspace	Bspace	DEL	-
16	0D	Tab	Ext	-	-
17	15	q	Q	DC1	ext
18	1D	w	W	ETB	ext
19	24	e	E	ENQ	ext
20	2D	r	R	DC2	ext
21	26	t	T	DC4	ext
22	35	y	Y	EM	ext
23	3C	u	U	NAK	ext
24	43	i	I	HT	ext
25	44	o	O	SI	ext
26	4D	p	P	DLE	ext
27	54	[	{	ESC	-
28	5B	]	}	GS	-
29	5D	\	|	FS	-
30	58	Caps Lk	-	-	-
31	16	a	A	SOH	ext
32	1B	s	S	DC3	ext
33	23	d	D	EOT	ext
34	2B	f	F	ACK	ext
35	34	g	G	BEL	ext
36	33	h	H	BS	ext
37	3B	j	J	LF	ext
38	42	k	K	VT	ext
39	4B	l	L	FF	ext
40	4C	;	:	-	-
41	52	'	"	-	-

56. AT 101-Key Keyboard (cont.)

Key #	Scan Code	Base Case	Upper Case	CTRL	ALT
43	5A	Enter	Enter	LF	-
44	12	Lt Shift	-	-	-
46	1A	z	Z	SUB	ext
47	22	x	X	CAN	ext
48	21	c	C	ETX	ext
49	2A	v	V	SYN	ext
50	32	b	B	STX	ext
51	31	n	N	SO	ext
52	3A	m	M	CR	ext
53	41	,	<	-	-
54	49	.	>	-	-
55	4A	/	?	-	-
57	59	Rt Shift	-	-	-
58	14	Lt Ctrl	-	-	-
60	11	Lt Alt	-	-	-
61	29	Space	Space	Space	Space
62	E0,11	Rt Alt	-	-	-
64	E0,14	Rt Ctrl	-	-	-
75	E0,70	Insert	-	-	-
76	E0,71	Delete	-	-	-
79	E0,6B	Lt Arrow	-	-	-
80	E0,6C	Home	-	-	-
81	E0,69	End	-	-	-
83	E0,75	Up Arrow	-	-	-
84	E0,72	Dn Arrow	-	-	-
85	E0,7D	PgUp	-	-	-
86	E0,7A	PgDn	-	-	-
89	E0,74	Rt Arrow	-	-	-
90	77	Num Lock	-	-	-
91	6C	pad 7	Home	-	-
92	6B	pad 4	Lt Arrow	-	-
93	69	pad 1	End	-	-
95	E0,4A	pad /	pad /	-	-
96	75	pad 8	Up Arrow	-	-
97	73	pad 5	-	-	-
98	72	pad 2	Dn Arrow	-	-
99	70	pad 0	Insert	-	-
100	7C	pad *	pad *	-	-
101	7D	pad 9	PgUp	-	-
102	74	pad 6	Rt Arrow	-	-
103	7A	pad 3	PgDn	-	-
104	71	pad .	Delete	-	-

56. AT 101-Key Keyboard (cont.)

Key #	Scan Code	Base Case	Upper Case	CTRL	ALT
105	7B	pad -	pad -	-	
106	79	pad +	pad +	-	-
108	E0,5A	pad Enter	pad Enter	-	-
110	76	Esc	Esc	-	-
112	05	F1	ext	ext	ext
113	06	F2	ext	ext	ext
114	04	F3	ext	ext	ext
115	0C	F4	ext	ext	ext
116	03	F5	ext	ext	ext
117	0B	F6	ext	ext	ext
118	83	F7	ext	ext	ext
119	0A	F8	ext	ext	ext
120	01	F9	ext	ext	ext
121	09	F10	ext	ext	ext
122	78	F11	ext	ext	ext
123	07	F12	ext	ext	ext
124	Note 1	PrtSc	-	-	-
125	7E	Scr Lk	-	-	-
126	Note 2		Pause-Break		

NOTES:
ext = extended (returns 00 followed by scan code)
Pause-Break = CTRL and Num Lock combination
Ctrl-Alt-Del = Warm Boot

Note 1: Print Screen Key: Down code, E0 12 E0 7C,
Up code, E0 F0 7C E0 F0 12
If Crtl down, Down code, E0 7C,
Up code E0 F0 7C
If Alt down, Down code, B4, Up code D0 B4

Note 2: Pause Key: Down code, E1 14 77 E1 F0 14 F0 77,
Up code, none
Break is active when Crtl is down:
Down code E0 7E E0 F0 7E, Up code, none

Keyboard information extracted from "PC Keyboard Design"
by Gary Konzak (Annabooks).
Also see this reference for the 101-key
XT Keyboard scan codes.

57. AT Keyboard Commands

The AT Keyboards can accept commands initiated by the system and sent through the 8042 keyboard controller.

Commands to Keyboard

Hex	Name	Description
F5	Default Disable	Resets all conditions to default state, stops scanning.
EE	Echo	Instruct KB to echo an EE code.
F4	Enable	KB replies with ACK, resumes scanning.
FE	Resend	KB resends last output.
FF	Reset	Resets KB.
F6	Set Default	Reset KB to default state.
F3	Set Typematic Rate/Delay	Set repeat and delay conditions for keys.
ED	Set/Reset Mode Indicators	Set or rest the LED's according to contents of following byte.
F2	Read ID code.	Tells KB to respond with 2-byte ID
F0	Select Scan Code Set	Tells KB which internal scan code set to use.
F7-FA	Set All Keys	Sets typematic and make/break operation of KB.
FB-FD	Set Key Types	Sets typematic and make/break operation for specific keys.

Commands to System

Hex	Name	Description
FA	ACK	Acknowledge to a command.
AA	Test OK	Internal Diagnostic OK.
F0	Break Prefix	Following scan code byte signifies key release.
FD	Diagnostic Failure	Internal diagnostic failed.
EE	Echo Response	Response to ECHO Command.
00 and FF	Error buffer	These two codes may indicate an overrun or an unidentified key.

58. ASCII Control Codes

Hex	Dec	Key	Name	Description
00	0	^@	NUL	Null
01	1	^A	SOH	Start of Header
02	2	^B	STX	Start of Text
03	3	^C	ETX	End of Text
04	4	^D	EOT	End of Transmission
05	5	^E	ENQ	Enquiry
06	6	^F	ACK	Acknowledge
07	7	^G	BEL	Bell
08	8	^H	BS	Backspace
09	9	^I	HT	Horizontal Tab
0A	10	^J	LF	Line Feed
0B	11	^K	VT	Vertical Tab
0C	12	^L	FF	Form Feed
0D	13	^M	CR	Carriage Return
0E	14	^N	SO	Shift Out
0F	15	^O	SI	Shift In
10	16	^P	DLE	Data Link Escape
11	17	^Q	DC1	Device Control 1
12	18	^R	DC2	Device Control 2
13	19	^S	DC3	Device Control 3
14	20	^T	DC4	Device Control 4
15	21	^U	NAK	Negative Acknowledge
16	22	^V	SYN	Synchronous Idle
17	23	^W	ETB	End Transmission Block
18	24	^X	CAN	Cancel
19	25	^Y	EM	End of Medium
1A	26	^Z	SUB	Substitute
1B	27	^[	ESC	Escape
1C	28	^\	FS	File Separator
1D	29	^]	GS	Group Separator
1E	30	^^	RS	Record Separator
1F	31	^_	US	Unit Separator

Key column refers to combination of CTRL key and specified key to generate control code.

see: UTF-8 first 128

59. Screen Codes

Dec	Hex	Sym.	Dec	Hex	Sym.
0	00		32	20	
1	01	^A	33	21	!
2	02	^B	34	22	"
3	03	^C	35	23	#
4	04	^D	36	24	$
5	05	^E	37	25	%
6	06	^F	38	26	&
7	07	^G	39	27	'
8	08	^H	40	28	(
9	09	^I	41	29	)
10	0A	^J	42	2A	*
11	0B	^K	43	2B	+
12	0C	^L	44	2C	,
13	0D	^M	45	2D	-
14	0E	^N	46	2E	.
15	0F	^O	47	2F	/
16	10	^P	48	30	0
17	11	^Q	49	31	1
18	12	^R	50	32	2
19	13	^S	51	33	3
20	14	¶	52	34	4
21	15	§	53	35	5
22	16	^V	54	36	6
23	17	^W	55	37	7
24	18	^X	56	38	8
25	19	^Y	57	39	9
26	1A	^Z	58	3A	:
27	1B	\	59	3B	;
28	1C	^\	60	3C	<
29	1D	^]	61	3D	=
30	1E	^^	62	3E	>
31	1F	^_	63	3F	?

59. Screen Codes (cont.)

Dec	Hex	Sym.	Dec	Hex	Sym.
64	40	@	96	60	`
65	41	A	97	61	a
66	42	B	98	62	b
67	43	C	99	63	c
68	44	D	100	64	d
69	45	E	101	65	e
70	46	F	102	66	f
71	47	G	103	67	g
72	48	H	104	68	h
73	49	I	105	69	i
74	4A	J	106	6A	j
75	4B	K	107	6B	k
76	4C	L	108	6C	l
77	4D	M	109	6D	m
78	4E	N	110	6E	n
79	4F	O	111	6F	o
80	50	P	112	70	p
81	51	Q	113	71	q
82	52	R	114	72	r
83	53	S	115	73	s
84	54	T	116	74	t
85	55	U	117	75	u
86	56	V	118	76	v
87	57	W	119	77	w
88	58	X	120	78	x
89	59	Y	121	79	y
90	5A	Z	122	7A	z
91	5B	[	123	7B	{
92	5C	\	124	7C	|
93	5D	]	125	7D	}
94	5E	^	126	7E	~
95	5F	_	127	7F	←

59. Screen Codes (cont.)

Dec	Hex	Sym.	Dec	Hex	Sym.
128	80	Ç	160	A0	á
129	81	ü	161	A1	í
130	82	é	162	A2	ó
131	83	â	163	A3	ú
132	84	ä	164	A4	ñ
133	85	à	165	A5	Ñ
134	86	å	166	A6	ª
135	87	ç	167	A7	º
136	88	ê	168	A8	¿
137	89	ë	169	A9	⌐
138	8A	è	170	AA	¬
139	8B	ï	171	AB	½
140	8C	î	172	AC	¼
141	8D	ì	173	AD	¡
142	8E	Ä	174	AE	«
143	8F	Å	175	AF	»
144	90	É	176	B0	▒
145	91	æ	177	B1	▓
146	92	Æ	178	B2	▓
147	93	ô	179	B3	│
148	94	ö	180	B4	┤
149	95	ò	181	B5	╡
150	96	û	182	B6	╢
151	97	ù	183	B7	╖
152	98	ÿ	184	B8	╕
153	99	Ö	185	B9	╣
154	9A	Ü	186	BA	║
155	9B	¢	187	BB	╗
156	9C	£	188	BC	╝
157	9D	¥	189	BD	╜
158	9E	₧	190	BE	╛
159	9F	ƒ	191	BF	┐

59. Screen Codes (cont.)

Dec	Hex	Sym.	Dec	Hex	Sym.
192	C0	└	224	E0	α
193	C1	┴	225	E1	ß
194	C2	┬	226	E2	Γ
195	C3	├	227	E3	π
196	C4	─	228	E4	Σ
197	C5	┼	229	E5	σ
198	C6	╞	230	E6	µ
199	C7	╟	231	E7	τ
200	C8	╚	232	E8	Φ
201	C9	╔	233	E9	Θ
202	CA	╩	234	EA	Ω
203	CB	╦	235	EB	δ
204	CC	╠	236	EC	∞
205	CD	═	237	ED	ø
206	CE	╬	238	EE	ε
207	CF	╧	239	EF	∩
208	D0	╨	240	F0	≡
209	D1	╤	241	F1	±
210	D2	╥	242	F2	≥
211	D3	╙	243	F3	≤
212	D4	╘	244	F4	⌠
213	D5	╒	245	F5	⌡
214	D6	╓	246	F6	÷
215	D7	╫	247	F7	≈
216	D8	╪	248	F8	°
217	D9	┘	249	F9	∙
218	DA	┌	250	FA	·
219	DB	▉	251	FB	√
220	DC	▄	252	FC	ⁿ
221	DD	▌	253	FD	²
222	DE	▐	254	FE	■
223	DF	▀	255	FF	

60. MS-DOS Commands

Append:	APPEND [[drive:]path[;...]] [/X[:ON|:OFF]][/PATH:ON|/PATH:OFF][/E]
Attribute:	ATTRIB[+R|-R][+A|-A][+S|-S][+H|-H][[drive:]path]filename][/s]
Backup:	See MSBACKUP
Run Program:	[drive:]filename[parameters]
Break:	BREAK [ON|OFF]
Change Code Page:	CHCP [nnn]
Change Directory:	CHDIR|CD [[drive:]path]|[..]
Check Disk:	CHKDSK [drive:][[path]filename][/F][/V]
Clear Screen:	CLS
Command:	COMMAND [[drive:]path][device][/E:nnnn][/Y[/C command | /K command]]
Compare Files:	COMP [[d:][path][filename]][[d:][path][filename]
Copy:	COPY [/Y | -Y][/A | /B] source [/A | /B] [+source[/A | /B] [+...]] [destination[/A | /B]] [/V]
Console:	CTTY device
Date:	DATE [[mm-dd-yy][[mm/dd/yy][[mm.dd.yy]]
Defrag:	DEFRAG [drive:] [/F] [/S[:]order] [/B] [/SKIPHIGH] [/LCD | /BW | /GO] [/H]
	DEFRAG [drive:] [/U] [/B] [/SKIPHIGH] [/LCD | /BW | /GO] [/H]
Delete:	DEL | ERASE [drive:] [path] filename [/P]
Delete Tree:	DELTREE [/Y] [drive:]path [[drive:]path[...]]
Directory:	DIR [drive:][path][filename][/P][/W] [/A[[attributes]]][/O[[:]sortorder]] [/S] [/B] [/L] [/C]
Disk Compare:	DISKCOMP [drive1: [drive2:]] [/1] [8]
Disk Copy:	DISKCOPY [drive1:[drive2:]] [/1] [/V] [/M]

Doskey:	DOSKEY [/REINSTALL] [/BUFSIZE = size] [/MACROS] [/HISTORY] [/INSERT | OVERSTRIKE] [macroname = [text]]
DOS Shell:	DOSSHELL [/T[:res[n]]] [/B] for text mode DOSSHELL [/G[:res[n]]] [/B] for graphics mode
Edit:	EDIT [[drive:] [path] filename] [/B] [/G] [/H] [/NOHI]
EMM386:	EMM386 [ON | OFF | AUTO] [W = ON | W = OFF] do not use when Windows is running
Erase:	ERASE | DEL [drive:][path]filename
Exe to Bin:	EXE2BIN [drive:]pathname1 [drive:]pathname2
Exit:	EXIT (return to previous level)
Expand:	EXPAND [drive:][path]filename [[drive:][path]filename [....]] destination
Fast Help:	FASTHELP [command] | [command] /?
Fastopen:	FASTOPEN drive: [[=]n] [drive:[[n][...]] [/X]
File Compare:	FC[/A][/C][/L][/LBn][/N][/nnnn][/T][/W][drive1:][path1]filename1[drive2][path2]filename2 (ASCII) FC[/B][drive1:][path1]filename1[drive2:][path2]filename2 (binary)
Fdisk:	FDISK [/STATUS]
Find:	FIND:[/C][/N][/V][/I] "string" [[drive:][path]filename [...]]
For:	FOR %variable IN (set) DO command [command-parameters] Note: See also Batch Commands
Format:	FORMAT drive: [/V[label]] [/Q] [/U] [/F:size] [/B | /S] [/C] FORMAT drive: [/V[label]] [/Q] [/U] [/T:tracks /N:sectors] [/B | /S] [/C] FORMAT drive: [/V[label]] [/Q] [/U] [/1] [/4] [/B | /S] [/C] FORMAT drive: [/Q] [/U] [/1] [/4] [/8] [/B | /S] [/C]
Graphics:	GRAPHICS [type] [[drive:] [path] filename] [/R] [/B] [/LCD] [/PRINTBOX:STD | PRINTBOX:LCD]

Help:	HELP [/B] [/G] [/H] [/NOHI] [topic]
Install:	INSTALL = [drive:][path]filename
Interlink:	INTERLNK [client[:] = [server] [:]]
Interserver:	INTERSVR [drive:[...]] [/X = drive:[...]] [/LPT:[n | address]] [/COM:[n | address]] [/BAUD:rate] [/B] [/V]
Load Graphics:	GRAFTABL[437|860|863|865]|/STA[TUS]]|[?]
Screen Print:	GRAPHICS[printer][profile][/R][/B][/LCD][/C][/F][/P port][/printbox:id]
Define KB:	KEYB [xx[, [yyy] [,drive:][path]filename]]] [/E] [/ID:nnn] Note: xx is Country and yyy is char set
Label:	LABEL [drive:][label]
Loadhigh:	LOADHIGH | LH [drive:][path][filename [parameters] LOADHIGH | LH [/L:region1[,minsize1] [;region2[minsize2]...] [/S]] [drive:][path]filename [parameters]
Loadfix:	LOADFIX [drive:][path]filename [program-parameters]
Make Dir:	MKDIR | MD [drive:][path]new-directory
Mem:	MEM [/CLASSIFY | .DEBUG | /FREE | /MODULE modulename] [/PAGE]]
Memmaker:	MEMMAKER [/B] [/SESSION] [/SWAP:drive] [/T] [/UNDO] [/W:n,m] Note: don't use with Windows running
Mode:	MODE LPTn[:][=COMn[:][80|132 (cols)][,[[RETRY=[E|B|R]]|[LINES={6|8}][,P]] MODE [40|80|BW40|BW80|CO40|CO80|MONO][25|43|50|R|L][,T (test)]n MODE COMn[:][110|150|300|1200|2400|4800|9600[,N|O|E[,7|8[,1|2[,P]]]] MODE CON [COLS=m][LINES=n][RATE=r][DELAY=d] MODE device CP [PREP=((cplist) filename)][SELECT=CP][/STATUS]
More:	MORE , [drive:][path]filename or command-name | MORE
Move:	MOVE [/Y | /-Y] [drive:][path]filename[,[drive][path]filename[...]]
MS Anti-Virus:	MSAV [drive:] [/S | /C] [/R] [/A | /L] [/N] [/P] [/F] [/VIDEO]

MS Backup:	MSBACKUP [setup_file] [/BW | LCD | /MDA] Note: this is not the same as Backup for Windows.
MS CD-ROM:	MSCDEX /D:driver [/D:driver2...] [/E] [/K] [/S] [/V] [/L:letter] {/M:number] Do not use after Windows starts
MS Details:	MSD [/I] [/F[drive:][path]filename] [/P[drive:][path]filename] [/S[drive:][path][filename]]
Natnl Language:	NLSFUNC [[drive:][path]filename[.ext]]
Path:	PATH [drive:]path[[;[drive:]path]...]
Power Mgmt:	POWER [ADV[:MAX | REG | MIN] | STD | OFF]
Print:	PRINT [/C:device] [/B:size] [/U:ticks1] [/M:ticks2] [/S:ticks3] [/Q:qsize] [/T] [[drive:][path]filename [...]] [/C] [/P]
Prompt:	PROMPT [text] (common usage is pg)
Qbasic:	QBASIC [/B] [/EDITOR] [/G] [/H] [/MBF] [/NOHI] [[/RIN]drive:][path]filename]
Recover:	RECOVER [drive:][path]filename]
Rename:	REN[AME][drive:][path]oldname newname
Replace:	REPLACE [drive1:][path1] filename [drive2:][path2][/A]/P]/R][/W]
	REPLACE [drive1:][path1] fileneme [drive2:][path2[/P][/R][/S][/W][/U]
Restore:	RESTORE drive1: drive2: [path[filename]] [/S] [/P] [/B:date] [/A:date][/E:time] [/L:time] [/M] /N] [/D:
Remove Dir:	RMDIR | RD [drive:][path]directory-name
ScanDisk:	SCANDISK [drive: [drive: ...] / ALL] [/CHECKONLY | /AUTOFIX [/NOSAVE] | /CUSTOM] [/SURFACE] [/MONO] [/NOSUMMARY]
Select:	SELECT[[drive1:]drive2:[path]] country keyboard
Set:	SET variable = [string]
Set Version	SETVER [[drive:path][filename n.nn] | [drive:path][filename [DELETE [/QUIET]]]
Share:	SHARE [/F:space][/L:locks]

SMARTDrive:	[drive:][path] SMARTDRV [/X] [[druve[+ | -]]...] [/R] [/C | /R] [/F | /N] [/L] [/V | /Q | /S] [/nitiCacheSize[/WinCacheSize2]] /ELElementSize] [/B:BufferSize]
	after SMARTDrive is running, use SMARTDRV[/S] [[drive[+ | -]] ...] [/C | /R] [/F | /N] [/Q | /S]
Sort:	SORT[/R][/+column] [<] [drive1:][path1]filename1 [> [drive2:][path2]filename2] or [command]] SORT [/R] [/+n] [>drive2:][path2]filename2]
Substitue:	SUBST[drive1][/D][[drive2:]path]]
System:	SYS [drive1:][path] drive2:
Time:	TIME [hours: [minutes[:seconds[.hundredths]]]] [/A | /P]
Tree:	TREE [drive:][path][/F][/A]
Type:	TYPE [drive:][path]filename
Undelete:	UNDELETE [[drive:][path]filename] [/DT | /DS | /DOS]
	UNDELETE [/LIST | /ALL | /PURGE [drive] | /STATUS | /LOAD | /UNLOAD | /S[drive] | /Tdrive[-entries]]
Unformat	UNFORMAT drive: [/L] [/TEST] [/P]
Version:	VER
Verify:	VERIFY [ON|OFF]
Volume:	VOL [drive:]
Vsafe:	VSAFE [/option[+ | -] ...] [/NE] [/NX] [/Ax | /Cx] [/N] [/D] [/U] Do not use when Windows is running.
Xcopy:	XCOPY source [destination][/Y | -Y] [/A /M][/DRIVE:mm-dd-yy][/E][/P][/S][/V][/W]

Call:	CALL [drive:][path] filename [batch parameters]
Choice	CHOICE [/C[:]keys] [/N][/S][/T[:]c,nn [text]
Display Text:	ECHO [ON|OFF] or ECHO [message]
For:	FOR %%variable IN (set) DO command [command-parameters]
Jump:	GOTO label
If:	IF [NOT] ERRORLEVEL number command
	IF [NOT] string1 == string2 command
	IF [NOT] EXIST filename command
Pause:	PAUSE [string]
Remark:	REM [string]
Shift:	SHIFT

Break:	BREAK = ON|OFF
Buffers:	BUFFERS = n [,m]
Country:	COUNTRY = xxxx[, [yyy][,[drive:][path] filename]]
Check State	CHKSTATE.SYS Note: This command is only used by MemMaker
Device:	DEVICE = [drive:][path]filename[dd-parameters]
Devicehigh	DEVICEHIGH [drive:][path]filename[dd-parameters]
Devicehigh	DEVICEHIGH [[/L.region1[,minsize1][;region2[,minsize2] [/S]] = [drive:][path]filename[dd-parameters]
ANSI	DEVICE = [drive:][path]ANSI.SYS [/X][/K][/R]
Display	DEVICE = [drive:][path]DISPLAY.SYS CON [:] =(type [,[hwcp][,n]])
Display	DEVICE = [drive:][path]DISPLAY SYS CON [:] =(type [,[hwcp][,(n,m)]])
Dblspace	DEVICE = [drive:][path] DBLSPACE.SYS /MOVE [/NOHMA]
Dblspace	DEVICEHIGH = [drive:][path] DBLSPACE.SYS /MOVE [/NOHMA]
Driver	DEVICE = [drive:][path]DRIVER.SYS /D:number [/C][/F:factor][/H:heads][/S:sectors] [/T:tracks]
EGA	DEVICE = [drive:][path] EGA.SYS
EMM386	DEVICE = [drive:][path]EMM386.EXE [ON | OFF | AUTO] [memory] [NUN = size] [W = ON | W = OFF] [Mx | FRAME = address | /Pmmmm] [Pn = address] [X = mmmm-nnnn] [I = mmmm-nnnn] [NOEMS] [NOVCPI] [HIGHSCAN] [VERBOSE] [WIN = mmmm-nnnn] [NOHI] [ROM = mmmm-nnnn] pNOMOVEXBDA] [ALTBOOT]

Himem	DEVICE = [drive:][path] HIMEM.SYS [A20CONTROL:ON | OFF] [/CPUCLOCK:ON | OFF] [/EISA] [/HMAMIN=m] [/INT15=xxxx] [/NUMHANDLES=n] [/MACHINE:xxxx] [/SHADOWRAM:ON | OFF] [/TESTMEM:ON | OFF] [/VERBOSE]
Interlink	DEVICE = [drive:][path] INTERLNK.EXE [/DRIVES:n] [/NOPRINTER] [/COM[:][n | address]] [/LPT[:] [n | ADDRESS]] [/AUTO] [/NOSCAN] [/LOW] [/BAUD:rate] [/V]
Power:	DEVICE = [drive:][path] POWER.EXE [ADV[:MAX | REG | MIN] |STD | OFF] [/LOW]
RAM Drive:	DEVICE = [drive:][path]RAMDRIVE.SYS [DiskSize SectorSize [NumEntries]]] [/E|/A]
Set Version:	DEVICE = [drive:][path] SETVER.EXE
SMARTDrv	DEVICE = [drive:][path] SMARTDRV.EXE /DOUBLE_BUFFER
Vdisk	DEVICE = [drive:][path]VDISK.SYS [text][bbb][text][sss][text][ddd][/E][:m]
Xmaem	DEVICE = [drive:][path]XMAEM.SYS...
Xma2ems	DEVICE = [drive:][path]XMA2EMS.SYS...
DOS	DOS = HIGH | LOW [,UMB | ,NOUMB]
	DOS = [HIGH, | LOW,] UMB | NOUMB
Driveparm	DRIVPARM = /D:number [/C][/F:factor][/H:heads][/I][/N][/S:sectors][/T:tracks]
Fcbs:	FCBS = x Note: x values from 1 through 255, default 4.
Files:	FILES = x Note: x value from 8 through 255, default 8.
Include	INCLUDE = blockname

Install	INSTALL = [drive:][path]filename [command-parameters]
Fastopen	INSTALL = [[dos-drive:]dos-path]FASTOPEN.EXE drive:[[=]n]
Keyb	INSTALL = [[dos-drive:]dos-path]KEYB.COM [xx[,[yyy] [,[drive:][path]filename]]] [/E] [/ID:nnn]
Share	INSTALL = [[drive:]path] SHARE.EXE [/F:space] [/L:locks]
Last Drive	LASTDRIVE = x Note: x ranges from A to Z
Menu Color	MENUCOLOR = x [,y]
Menu Default	MENUDEFAULT = blockname [,timeout]
Menu Item	MENUITEM = blockname [,menu_text]
Numlock	NUMLOCK = [ON | OFF]
Remark	REM | ; [string] Note: Semicolon not for use in batch files
Set:	SET variable = [string]
Shell:	SHELL = [[dos-drive:]dos-path] COMMAND.COM [[drive:]path][device][/E:nnnn] [/P[/MSG]]]
	SHELL = [[drive:]path]filename [parameters]
Stacks:	STACKS = number,size Note: n from 8 through 64, s from 32 through 512.
Submenu	SUBMENU = blockname [,menu_text]
Switches	SWITCHES = /F /K /N /W

63. DEBUG Commands

Starting:	DEBUG [d:][path][filename][parm1][parm2]
Ending:	Q
Assemble:	A[address]
Compare:	C range address
Dump:	D[address] or D[range]
Enter:	E address [list]
Fill:	F range list
Go:	G[=address][break0][..break9]]
Hexmath:	H value1 value2
Input:	I port
Load:	L [address[drive, sector#, # of sectors]]
Move:	M range address
Name:	N filespec [parameter...]
Output:	O port byte
Proceed:	P [=address][number]
Quit:	Q
Register:	R [F]][registername]
Search:	S range list
Trace:	T [=address][number]
Unassemble:	U [address] or U [range]
Write:	W [address [drive, sector#, # of sectors]]

S F000:C000, FFFF "COM1_"
55, AA

64. MS-DOS Keystrokes

Reset:	Ctrl-Alt-Del (Warm Boot)
Stop Scroll:	Ctrl-Num Lock or Ctrl-S
Resume Scroll:	Any Key
Print Screen:	Shift-Prt Sc (Screen dump)
Print Screen:	Ctrl-Prt Sc (Continous)
End Operation:	Ctrl-Break or Ctrl-C
Next Line:	Ctrl-Enter (without CR)
Cancel Line:	Esc

65. Floppy Disk Formats
3.5" Diskettes

Formatted Capacity	720K	1.44MB	2.88MB
# of heads (Sides)	2	2	2
# of Cyls (Tracks)	80	80	80
# of Sectors/Track	9	18	36
Total # of Sectors	1440	2880	5760
# of Free Sectors	1426	2847	5726
# Sectors/Cluster	2	1	2
Total # of Clusters	713	2847	2863
# Sectors/FAT	3	9	9
# of FAT Copies	2	2	2
# of Root Dir Sectors	7	14	15
# Reserved Sectors	1	1	1
# of Hidden Sectors	0	0	0
# of Bytes/Sector	512	512	512
# of Bytes/Cluster	1024	512	1024
# Root Dir Entries	112	224	240
Media Descriptor	F9	F0	F0
Recorded Density	Double	High	High
DOS Version Began	3.20	3.30	5.00
DRIVER.SYS Switch	/F:2	/F:7	/F:9
FORMAT.EXE Switch	/F:720	/F:1.44	/F:2.88
Change-Line Support	YES	YES	YES

63. Floppy Disk Formats (cont.)
5.25" Diskettes

Formatted Capacity	160K	180K	320K	360K	1.2MB
# of heads (Sides)	1	1	2	2	2
# of Cyls (Tracks)	40	40	40	40	80
# of Sectors/Track	8	9	8	9	15
Total # of Sectors	320	360	640	720	2400
# of Free Sectors	313	351	630	708	2371
# Sectors/Cluster	1	1	2	2	1
Total # of Clusters	313	351	315	354	2371
# Sectors/FAT	1	2	1	2	7
# of FAT Copies	2	2	2	2	2
# of Root Dir Sectors	4	4	7	7	14
# Reserved Sectors	1	1	1	1	1
# of Hidden Sectors	0	0	0	0	0
# of Bytes/Sector	512	512	512	512	512
# of Bytes/Cluster	512	512	1024	1024	512
# Root Dir Entries	64	64	112	112	224
Media Descriptor	FE	FC	FF	FD	F9
Recorded Density	Double	Double	Double	Double	High
DOS Version Began	1.00	2.00	1.10	2.00	3.00
DRIVER.SYS Sw.	/F:0	/F:0	/F:0	/F:0	/F:1
FORMAT.EXE Sw.	/F:160	/F:180	/F:320	/F:360	/F:1.2
Change-Line Support	NO	NO	NO	NO	YES

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